Bit Plane Encoder (BPE)

SOURCE CONTROL DRAWING (SCD)

ASIC Design
Radiation Hardened

Revision – 2.1
January 27, 2011

Suggested Sources of Supply

AFX PART NUMBER	PROCURED PART NUMBER	PART MANUFACTURER	CAGE CODE
XS027A	2120326 / Bit Plane Encoder (BPE)	Aeroflex Colorado Springs, Inc. Colorado Springs, CO. 80907	65342

CAUTION:

THIS DEVICE IS STATIC SENSITIVE AND SHOULD BE SUBJECT TO SPECIAL HANDLING REQUIREMENTS.

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1.0 SCOPE

This drawing defines the requirements for the Bit Plane Encoder (BPE), an image compression, radiation hardened ASIC for use in space flight applications. The part shall be manufactured and tested in accordance with the space application (also known as Class S-like) requirements. The part shall have a minimum total dose radiation hardness of 50K Rad(Si).

1.1 STANDARD DEVICE TYPES

PURCHASER PART NUMBER	RELIABILITY LEVEL	REQ'D ASSEMBLY PROCESS	REQ'D SCREENING & QUALIFICATION	DIE PART NUMBER
2120326-01	Flight, Class S-Like	SECTION 3.0	SECTION 4.0	BPE XS027
2120326-02	PROTOTYPE	SECTION 3.0	SECTION 4.0	BPE XS027

2.0 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the date of request for quotation apply to the extent specified herein. In the event of a conflict between this specification and the listed documents, this specification shall govern.

Military Specifications

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for

Military Standards

MIL-STD-883	Microelectronics, Test Methods and Procedures for
MIL-STD-1580	Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts

Non-Government publications

Functional Specification	BPE Specification
Statement of Work	Revision 4 dated 5/6/2009

3.0 REQUIREMENTS

3.1 General

The individual item requirements for device class S-like shall be in accordance with this source control drawing and as specified herein.

3.2 Wafer Lot

All parts delivered on any purchase order to this drawing must come from one wafer lot

3.3 Lot Date Code

Unless otherwise authorized by the purchaser in writing, all parts supplied to the requirement of this drawing on a single purchase order line item shall be from the same lot/date code shall consist of a unique, four digit minimum, numeric or alphanumeric code that represents a class S-like inspection lot.

3.4 Absolute Maximum Ratings

Absolute maximum ratings shall be as specified in Table 1, herein.

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	-65 to +150	^oC
T_A	Operating Temperature	-55 to +125	^oC
V_{DDmax}	Max. voltage between V_{DD} and V_{SS}	-0.25 to +2.75	volts
$V_{DVDDmax}$	Max. voltage between V_{DVDD} and V_{DVSS}	-0.3 to +3.6	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DVDD}+0.3	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{DVSS}-0.3	volts
Fmax	Maximum frequency	20	MHz

3.5 Recommended Operating Conditions:

Recommended Operating Conditions shall be as specified in Table 2, herein.

Table 2: Recommended Operating Conditions

Symbol	Parameter	Range	Units
T_A	Operating Temperature	-55 to +125	^oC
V_{DD}	Standard Operating voltage V_{DD}	2.25 to +2.75	volts
V_{DVDD}	Standard Operating voltage V_{DVDD}	3.0 to +3.6	volts

3.6 Electrical Characteristics

Electrical performance characteristics shall be as specified in Table 3, herein. The devices shall operate over the specified temperature range. AC characteristics are specified in Table 4.

3.7 Power up sequence

The VDD power must be applied either before or during of the initial application of the DVDD

Table 3: Electrical Performance Characteristics

Symbol	Parameter	Min	Max	Units	Conditions /1
VIH(min)	Min. High Level Input Voltage	0.7 * V_{DVDD}	-	volts	Guaranteed Logic '1'
VIL(max)	Max. Low Level Input Voltage	-	0.3 * V_{DVDD}	volts	Guaranteed Logic '0'
VIHC(min)	Min. High Level Input Voltage, High CLOCK Input	0.7 * V_{DVDD}	-	volts	Guaranteed Logic '1'
VILC(max)	Max. Low Level Input Voltage, Low CLOCK Input	-	0.3 * V_{DVDD}	volts	Guaranteed Logic '0'
VOH(min)	Min. High Level Output Voltage High	2.35	-	volts	IOH = -30.0 ma
VOH(min)	Min. High Level Output Voltage High	2.7	-	volts	IOH = -4.0 ma
VOL(max)	Max. Low Level Output Voltage Low	-	0.6	volts	IOH = -30.0 ma
VOL(max)	Max. Low Level Output Voltage Low	-	0.4	volts	IOH = -4.0 ma
IIH	High Level Input Leakage Current	-1	1	µA	Vin = V_{DVDD}
IIL	Low Level Input Leakage Current	-1	1	µA	Vin = V_{DVSS}
$I_{MAXQFMAX}$ 1/	Maximum quiet (core) VDD current at maximum frequency	-	420	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Randomall
		-	250	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = p3t1
		-	225	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = te1
		-	225	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = te2
		-	225	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = te4
		-	765	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Scan
$I_{MAXDFMAX}$	Maximum dirty (I/O) VDD current at maximum frequency	-	350	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Randomall
		-	20	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = p3t1
		-	1	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = te1
		-	1	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = te2
		-	1	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = te4
		-	280	mA	f_{CLK} = 20MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Scan
I_{MAXQDC}	Maximum quiet (core) VDD current at DC (no clock)	-	120	uA	T_A = -55°C , +25°C
		-	15	mA	T_A = +125°C
$I_{MAXQDCPR}$ 2/	Maximum quiet (core) VDD current at DC (no clock) Post Radiation	-	600	uA	50 Krads total dose at a dose rate between 15 mrad(Si)/sec and 30 mrad(Si)/sec.
I_{MAXDDC}	Maximum dirty (I/O) VDD current at DC (no clock)	-	10	uA	T_A = -55°C , +25°C
		-	25	uA	T_A = +125°C

$I_{MAXDDCPR}$ 2/	Maximum dirty (I/O) VDD current at DC (no clock) Post Radiation	-	300	uA	50 Krads total dose at a dose rate between 15 mrad(Si)/sec and 30 mrad(Si)/sec.

1/: Operating Conditions: V_{DVDD} = 3.3V ± 10%, V_{DVSS} = 0V, V_{DD} = 2.5V ±10%, V_{SS} = 0V, T_A = -55°C to +125°C, unless otherwise specified.
2/ Temp = 25C

Table 4: AC Characteristics 1/

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{RST} 2/	RESETN pulse width low	10		cycles	CLK and SCC on
t_{CLK0} 2	CLK zero time	20		ns	f_{CLK} = 20MHz
t_{CLK1} 2/	CLK one time	20		ns	f_{CLK} = 20MHz
t_{SCC0} 2/	SCC zero time	20		ns	f_{SCC} = 20MHz
t_{SCC1} 2/	SCC one time	20		ns	f_{SCC} = 20MHz
t_{ALE0} 2/	ALE zero time	20		ns	f_{ALE} = 20MHz
t_{ALE1} 2/	ALE one time	20		ns	f_{ALE} = 20MHz
t_{SSU} 3/	SCE, SCD setup to rising SCC	10		ns	f_{SCC} = 20MHz
t_{SHD} 3/	SCE, SCD hold to rising SCC	0		ns	f_{SCC} = 20MHz
t_{PSU} 3/	PIEN, PWRN, PRDN, and PIO setup to rising ALE_CLK	5		ns	f_{ALE} = 20MHz
t_{PHD} 3/	PIEN, PWRN, PRDN, and PIO hold to rising ALE_CLK	2		ns	f_{ALE} = 20MHz
t_{SU}	DVALID, DEOI, and D setup to rising CLK	15		ns	f_{CLK} = 20MHz
t_{HD}	DVALID, DEOI, and D hold to rising CLK	0		ns	f_{CLK} = 20MHz
t_{QV}	QRDY, Q, QSOS, QEOS, QRTRIG, and QFILL output delay from rising CLK		12	ns	Load = 50pF max

1/ Operating Conditions: V_{DVDD} = 3.3V ± 10%, V_{DVSS} = 0V, V_{DD} = 2.5V ±10%, V_{SS} = 0V, T_A = -55°C to +125°C
2/ Guaranteed by simulation; not physically tested
3/ These timings subsume timings in the BPE functional specification (see Figures 1, 2, 3, 4):
t_{SSU} includes t_{SESU} and t_{SDSU}
t_{SHD} includes t_{SEHD} and t_{SDHD}
t_{PSU} includes t_{IESU}, t_{WLSU}, t_{RLSU}, t_{PDSU}
t_{PHD} includes t_{IEHD}, t_{WLHD}, t_{RLHD}, t_{PDHD}

Figure 1: PRDN timing

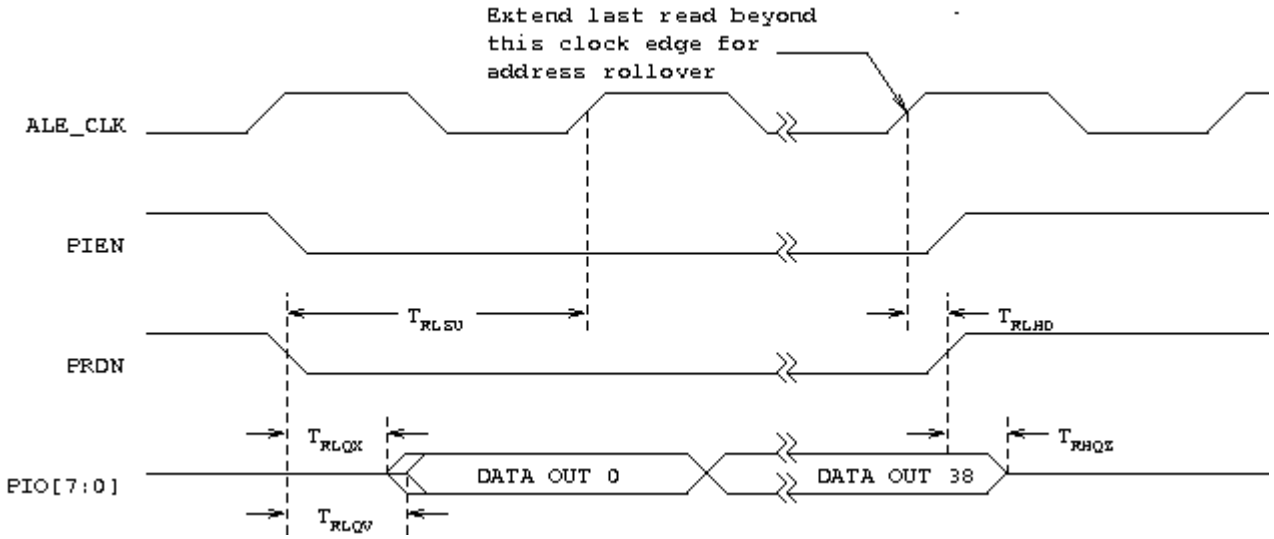


Figure 2: PIEN, PWRN, and PIO timing

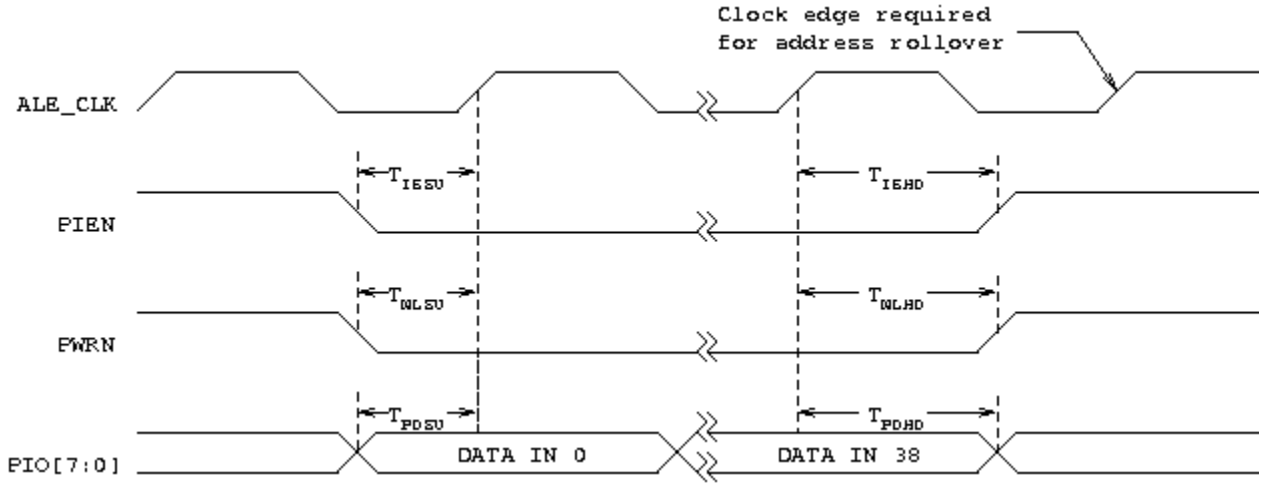


Figure 3: SCE and SCD timing

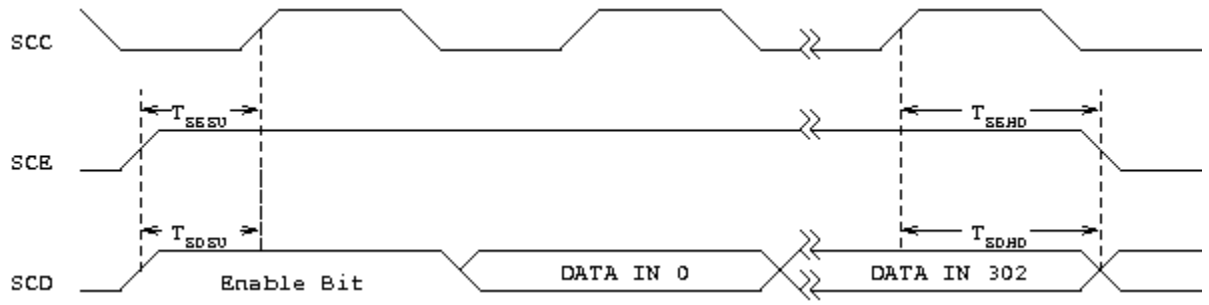
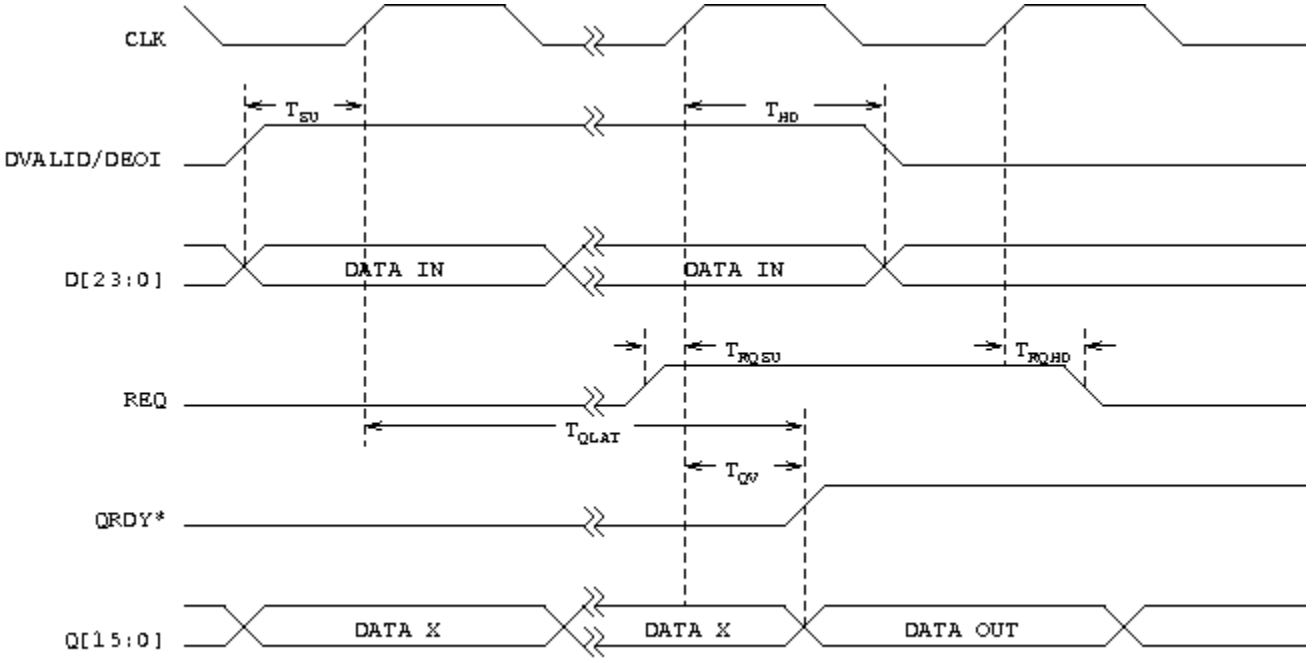


Figure 4: DVALID, D, DEOI, and Q output timing



3.8 Burn-In and Life Test Circuits

The burn-in and life test duration, test condition and test temperature, Should be as specified as here in The test circuit shall specify the inputs, outputs, biases and power dissipation, as applicable, in accordance with the intent specified in MIL-STD-883, Methods 1015 and 1005. See burn-in diagram, Figure 5.

3.9 Mechanical Characteristics

3.9.1 Design, Construction, and Physical Characteristics

In accordance with Table 8 and Figure 6.

3.10 Marking

In accordance with MIL-PRF-38535 and the following:

3.10.1 Part Marking Requirement, Class Level S-like

2120326-001 (2)
ARXX (3) BPE_XS027A (4)
USA (5) YYWWA (6)
Δ(1) YYWW (7) 0ABCA (8)
XXX (9)

(1) Pin 1 indicator and ESD identifier
(2) Customer part number
(3) Aeroflex trademark, Name, or Symbol
(4) Aeroflex part identification code
(5) Country of origin
(6) Inspection lot code
YYWW = Inspection lot code
A = Inspection sublot(s)
(7) Seal week
YY = Last two digits of the year the assembly lot was sealed
WW = The work week that the assembly lot was sealed
(8) Assembly Lot number
(9) Serial number

3.10.2 Part Marking Requirement, Prototype

Proto(6)
2120326-002(2)
ARXX (3) BPE_XS027A (4)
USA (5) YYWW (7)
Δ(1) 0ABCA (8)

(1) Pin 1 indicator and ESD identifier
(2) Customer part number
(3) Aeroflex trademark, Name, or Symbol
(4) Aeroflex part identification code
(5) Country of origin
(6) Device type
(7) Seal week
YY = Last two digits of the year the assembly lot was sealed
WW = The work week that the assembly lot was sealed
(8) Assembly Lot number

3.11 Serialization

When specified in the purchase order, prior to the first recorded electrical measurement in screening, each microcircuit shall be marked with a unique serial number assigned consecutively within the level of the individual microcircuit within that inspection lot.

3.12 Radiation Hardness Assurance

When tested as specified in Appendix B and C of MIL-PRF-38535 and in accordance with Method 1019, Condition C of MIL-STD-883, the part shall meet a total ionization radiation dose of 50K Rad(Si), RHA level L.

3.12.1 Traceability

Inspection lot records shall be maintained to provide traceability from the device serial number to the specific wafer lot or to the specific wafer when testing to any Group E subgroup is performed on a wafer by wafer basis.

3.12.2 RLAT and LATCH-UP Testing.

Validation complete by CAMBR laboratory testing to 100Krad min. Latch up testing passed to LET 120 Mev cm2 / mg .

3.13 Environmental Testing

The device shall meet the requirements of this drawing following exposure to any singular or natural combination of the environmental conditions specified in the quality assurance provisions of this document.

3.14 Workmanship

The devices shall be processed in such a manner as to be uniform in quality and shall be free from any defects that would adversely affect life, serviceability or appearance.

3.15 Wafer Lot Acceptance

ICs LLC OF McCALL IDAHO Is Source of Wafers/Dice. Recommended Manufacturing Foundry Shall be TSMC-WAFERTECH LLC, CAMAS, WA. . The wafer lot shipped for Assembly processes should be accompanied by a copy of Certification Of Conformance. The wafer lot should be 1st optical inspected and wafer probed as the wafer lot acceptance of receipt prior to Assembly processes.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Prototype Screening

Prototype devices will be processed per manufacturer's standard prototype flow. Additional requirements if any shall be documented in the purchase order.

4.2 Sampling and inspection

Sampling and inspection procedures shall be in accordance with Table 5.

4.3 Screening

Screening shall be in accordance with Table 5 'and shall be conducted on all devices prior to qualification and technology conformance inspection.

Table 5: Lot Screening Flow

Screen	Class Level S-Like
	Method
Wafer Lot Acceptance	---
Non-Destructive Bond Pull	2023; In-line SPC alternative
Precap Visual	2010, Cond A
Temperature Cycling	1010 Cond C
Constant Acceleration	2001
Particle Impact Noise Detection (PIND)	2020, Cond A
Seal Test (Fine /Gross Leak)	1014
Radiography	2012
Pre Burn-in Electrical	Applicable specification
Dynamic Burn-in	1015
Interim Electrical Test	Applicable specification
Percent Defective Allowable (PDA)	PDA 5%, 3% for Functional
Final Electrical Test	Applicable specification
External Visual Inspection	2009

4.4 Qualification inspection

Qualification inspection shall be in accordance with the source control drawing. Inspections to be performed shall be group A, group C, package first article evaluation and group E inspections (see 4.4.1 through 4.4.4).

TABLE 6: Electrical Test Requirements

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)
Interim electrical parameters (see 4.2)	- - -
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7 add 2, 3, 8 9, 10 & 11
Group D end-point electrical parameters (see 4.4)	1, 7
Group E end-point electrical parameters (see 4.4)	- - -

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

Per MIL-STD-883, Test Method 5005, in-line alternative

4.4.2 Group C Inspection.

The group C inspection end-point electrical parameters shall be as specified in table 6 herein. The steady-state life test duration, test condition and test temperature shall be in accordance with test method 1005 of MIL-STD-883.. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883. Group C sample size is 12 parts.

4.4.3 Group D inspection.

The group D package test will be performed as first article functional evaluation test. A 16 piece sample will be subjected to a simulated package assembly flow and will be subjected to 40 temperature cycles, centrifuge, and fine & gross leak test before being submitted to the test listed in the following table:

Table 7: Package First Article Functional Evaluation

Evaluation /Test	Test conditions	Sample plan	Criteria / Notes
Thermal Series Evaluation	Per M5005, D-3 15 Thermal Shocks 100 Temperature cycles Fine/Gross leak test	15/0	Per Mil-Std-883, M5005, D-3 test requirements
Salt Atmosphere	Per M1009, Cond A	15/0	Visual Inspection per M1009
Physical Dimensions	Per M2016	2/0	Per Package drawing
Solderability	Per M2003	22/0 Sample 22 leads from 3 devices	Solder temperature 245˚C +/- 5˚C

4.4.4 Group E Inspection.

Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.13 herein). RHA levels for device class S-Like shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table 6 herein.

4.4.5 Total Dose Irradiation Testing.

Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition C. Sample size is 5 parts and taken from Group C samples after completion of group C testing. The Group E testing will be performed at a dose rate between 15 mrads(Si)/sec and 30mrad(Si)/sec to a total dose of 50 Krad (Si).

4.5 Destructive Physical Analysis

DPA will be performed by NASA.

4.6 Failure Analysis

Catastrophic failures (i.e. shorts or opens measurable or detectable at 25°C) subsequent to burn-in shall be analyzed. Reporting of failure and documentation of the analysis shall be in accordance with the provisions of the purchase order.

4.7 Inspection Verification

The customer reserves the right to witness testing, as specified in the procurement document, and prior to shipment will verify that all requirements of the purchase order and this specification have been satisfied.

4.7.1 Customer Source Inspection

When source inspection is specified in the procurement document, the supplier shall notify the customer's procuring agent FIVE days in advance of shipment so that appropriate planning can be made. The supplier shall make available in-process manufacturing, acceptance tests and other related documentation for the microcircuit lot submitted for final inspection for acceptance. Pre Cap source inspection is required.

4.8 Deliverable Data Items

The supplier's standard Class S-like data package shall be delivered with the devices under procurement for the inspection lot and as a minimum consists of the following:

a. 100% lot screening summary with in-line group A.
b. Radiography report.
c. Group C report (wafer lot or inspection lot specific, as applicable).
d. Package First Article Functional Evaluation report
e. Group E data, as applicable.
f. Variables data for pre-burn-in 25˚C and post-burn-in dynamic electrical tests (25˚C, 125˚C and -55˚C)
g. Variable data for post life test electrical tests (25˚C, 125˚C and -55˚C)
h. Certificate of Conformance
i. Failure Analysis Report, if applicable.

4.8.1 Correlation of Parts and Data Items

Parts delivered in each shipment shall be identified (e.g., individual unit packaging, tagging, or sticker affixed to part) so that data is identifiable to the individual parts contained in the shipment.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging

In accordance with MIL-PRF-38535.

5.2 Package Marking

The first level protective package shall be marked with the device part number, lot date code, serial number[s] and supplier name or identification. Higher level packaging shall include the above marking plus the purchase order number. The purchase order number must appear on the outermost package.

5.3 Special Handling Labels

Special handling labels shall be affixed to the exterior of the shipping containers to indicate that the contents are ESD sensitive.

6.0 ORDERING INFORMATION

As applicable, Customer Procurement Documents shall specify the following:

- This document and revision number
- Additions, deletions, and exceptions to this document
- Microcircuit Part Number
- DPA Requirements
- Failure Analysis Report
- Customer Source Inspection Requirements

Table 8: Device Pin-out

PIN	FUNCTION	I/O TYPE
1	VDD	
2	VSS	
3	RADDB_20	CMOS Output
4	NC	
5	RADDB_19	CMOS Output
6	NC	
7	NC	
8	RADDB_18	CMOS Output
9	RADDB_16	CMOS Output
10	RADDB_17	CMOS Output
11	NC	
12	RADDB_15	CMOS Output
13	NC	
14	RADDB_14	CMOS Output
15	RADDB_13	CMOS Output
16	RADDB_12	CMOS Output
17	RADDB_10	CMOS Output
18	NC	
19	RADDB_11	CMOS Output
20	RADDB_9	CMOS Output
21	DVDD	
22	DVDD	
23	DVSS	
24	NC	
25	RADDB_8	CMOS Output
26	RADDB_7	CMOS Output
27	RADDB_6	CMOS Output
28	RADDB_4	CMOS Output
29	RADDB_5	CMOS Output
30	RADDB_3	CMOS Output
31	DVDD	
32	RADDB_1	CMOS Output
33	RADDB_2	CMOS Output
34	RIOA_23	CMOS IN-OUT
35	RADDB_0	CMOS Output
36	RIOA_22	CMOS IN-OUT
37	NC	
38	RIOA_21	CMOS IN-OUT
39	RIOA_20	CMOS IN-OUT
40	RIOA_19	CMOS IN-OUT
41	VDD	
42	VDD	
43	VSS	
44	RIOA_18	CMOS IN-OUT
45	RIOA_16	CMOS IN-OUT
46	RIOA_17	CMOS IN-OUT
47	RIOA_15	CMOS IN-OUT
48	DVDD	
49	RIOA_14	CMOS IN-OUT
50	RIOA_12	CMOS IN-OUT
51	RIOA_13	CMOS IN-OUT
52	RIOA_10	CMOS IN-OUT
53	RIOA_11	CMOS IN-OUT
54	DVDD	
55	RIOA_9	CMOS IN-OUT

PIN	FUNCTION	I/O TYPE
56	RIOA_7	CMOS IN-OUT
57	RIOA_8	CMOS IN-OUT
58	RIOA_6	CMOS IN-OUT
59	VDD	
60	RIOA_5	CMOS IN-OUT
61	RIOA_3	CMOS IN-OUT
62	RIOA_4	CMOS IN-OUT
63	DVDD	
64	DVSS	
65	VDD	
66	VSS	
67	RIOA_2	CMOS IN-OUT
68	RIOA_1	CMOS IN-OUT
69	RNCSA	CMOS Output
70	RIOA_0	CMOS IN-OUT
71	RNOEA	CMOS Output
72	RNWEA	CMOS Output
73	DVDD	
74	RADDA_22	CMOS Output
75	RADDA_23	CMOS Output
76	RADDA_21	CMOS Output
77	RADDA_20	CMOS Output
78	RADDA_19	CMOS Output
79	RADDA_18	CMOS Output
80	DVDD	
81	RADDA_16	CMOS Output
82	RADDA_17	CMOS Output
83	RADDA_15	CMOS Output
84	NC	
85	RADDA_14	CMOS Output
86	DVDD	
87	DVSS	
88	RADDA_12	CMOS Output
89	RADDA_13	CMOS Output
90	VDD	
91	RADDA_11	CMOS Output
92	RADDA_9	CMOS Output
93	RADDA_10	CMOS Output
94	RADDA_7	CMOS Output
95	RADDA_8	CMOS Output
96	VDD	
97	RADDA_6	CMOS Output
98	NC	
99	NC	
100	DVDD	
101	RADDA_5	CMOS Output
102	RADDA_4	CMOS Output
103	RADDA_3	CMOS Output
104	VDD	
105	VDD	
106	VDD	
107	VSS	
108	RADDA_1	CMOS Output
109	RADDA_2	CMOS Output
110	DVDD	

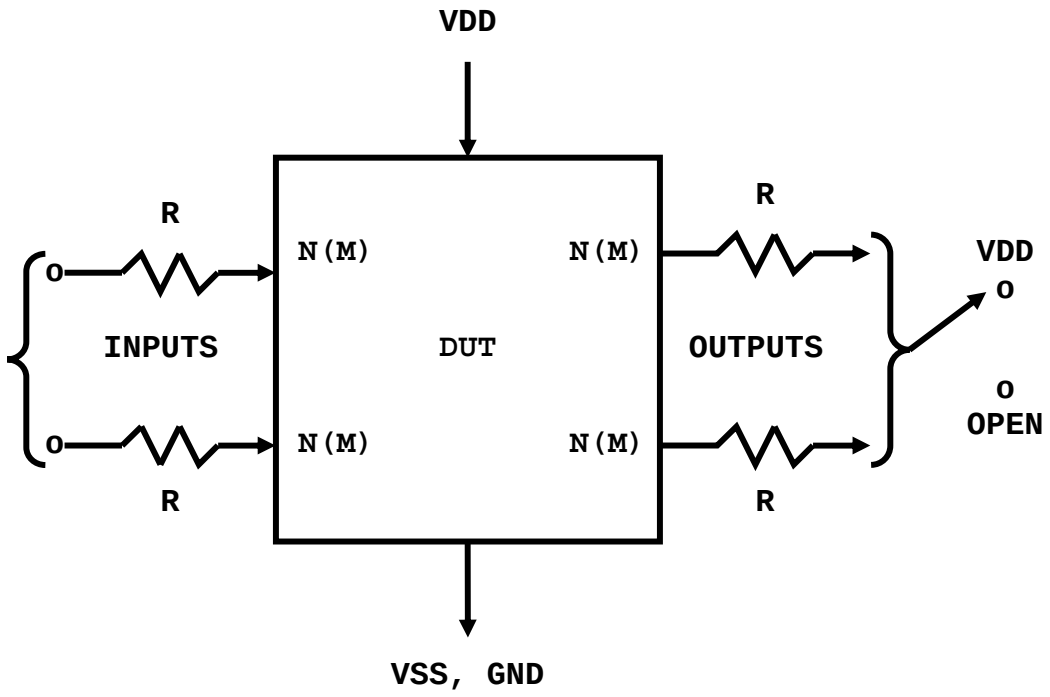
PIN	FUNCTION	I/O TYPE
111	RADDA_0	CMOS Output
112	VDD	
113	D_1	CMOS Input
114	D_0	CMOS Input
115	D_2	CMOS Input
116	D_3	CMOS Input
117	D_4	CMOS Input
118	D_5	CMOS Input
119	D_6	CMOS Input
120	D_8	CMOS Input
121	D_7	CMOS Input
122	D_9	CMOS Input
123	D_10	CMOS Input
124	D_11	CMOS Input
125	D_12	CMOS Input
126	D_13	CMOS Input
127	DVDD	
128	DVSS	
129	VDD	
130	VSS	
131	D_15	CMOS Input
132	D_14	CMOS Input
133	D_16	CMOS Input
134	NC	
135	D_17	CMOS Input
136	D_18	CMOS Input
137	D_19	CMOS Input
138	D_20	CMOS Input
139	D_21	CMOS Input
140	D_22	CMOS Input
141	D_23	CMOS Input
142	DVALID	CMOS Input
143	SOS	CMOS Output
144	DEOI	CMOS Input
145	EOS	CMOS Output
146	NC	
147	EOIS	CMOS Output
148	DVDD	
149	PMODE	CMOS Input
150	DVDD	
151	DVSS	
152	PUMODE	CMOS Input
153	PIEN	CMOS Input
154	PWRN	CMOS Input
155	PIO_0	CMOS IN-OUT
156	PRDN	CMOS Input
157	PIO_2	CMOS IN-OUT
158	DVDD	
159	PIO_1	CMOS IN-OUT
160	CLK	CMOS Input
161	VDD	
162	PIO_3	CMOS IN-OUT
163	PIO_4	CMOS IN-OUT
164	PIO_6	CMOS IN-OUT
165	PIO_5	CMOS IN-OUT
166	PIO_7	CMOS IN-OUT
167	ALE_CLK	CMOS Input

PIN	FUNCTION	I/O TYPE
168	DVDD	
169	PACK	CMOS Output
170	VDD	
171	VSS	
172	SCC	CMOS Input
173	PUPD	CMOS Input
174	SCE	CMOS Input
175	TE	CMOS Input
176	SCD	CMOS Input
177	VDD	
178	RESETN	CMOS Input
179	REQ	CMOS Input
180	QFILL	CMOS Output
181	QEOS	CMOS Output
182	QRTRIG	CMOS Output
183	QSOS	CMOS Output
184	DVDD	
185	QRDY	CMOS Output
186	Q_14	CMOS Output
187	Q_15	CMOS Output
188	Q_12	CMOS Output
189	Q_13	CMOS Output
190	DVDD	
191	DVDD	
192	DVSS	
193	VDD	
194	VSS	
195	Q_10	CMOS Output
196	Q_11	CMOS Output
197	Q_8	CMOS Output
198	Q_9	CMOS Output
199	Q_6	CMOS Output
200	Q_7	CMOS Output
201	Q_5	CMOS Output
202	DVDD	
203	Q_3	CMOS Output
204	Q_4	CMOS Output
205	Q_1	CMOS Output
206	Q_2	CMOS Output
207	Q_0	CMOS Output
208	DVDD	
209	RIOB_23	CMOS IN-OUT
210	RIOB_22	CMOS IN-OUT
211	RIOB_21	CMOS IN-OUT
212	NC	
213	NC	
214	DVDD	
215	DVSS	
216	VDD	
217	RIOB_19	CMOS IN-OUT
218	RIOB_20	CMOS IN-OUT
219	RIOB_18	CMOS IN-OUT
220	RIOB_17	CMOS IN-OUT
221	NC	
222	RIOB_16	CMOS IN-OUT
223	NC	
224	VDD	

PIN	FUNCTION	I/O TYPE
225	NC	
226	RIOB_15	CMOS IN-OUT
227	RIOB_14	CMOS IN-OUT
228	RIOB_13	CMOS IN-OUT
229	RIOB_12	CMOS IN-OUT
230	NC	
231	VDD	
232	NC	
233	RIOB_11	CMOS IN-OUT
234	VDD	
235	VSS	
236	RIOB_10	CMOS IN-OUT
237	RIOB_9	CMOS IN-OUT
238	RIOB_8	CMOS IN-OUT
239	RIOB_7	CMOS IN-OUT
240	RIOB_6	CMOS IN-OUT
241	DVDD	

PIN	FUNCTION	I/O TYPE
242	RIOB_5	CMOS IN-OUT
243	RIOB_4	CMOS IN-OUT
244	RIOB_3	CMOS IN-OUT
245	RIOB_2	CMOS IN-OUT
246	RIOB_1	CMOS IN-OUT
247	RIOB_0	CMOS IN-OUT
248	DVDD	
249	RNWEB	CMOS Output
250	RNOEB	CMOS Output
251	RADDB_23	CMOS Output
252	RNCSB	CMOS Output
253	RADDB_21	CMOS Output
254	RADDB_22	CMOS Output
255	DVDD	
256	DVSS	

Figure 5: Burn-In Diagrams



Notes:

1. For Dynamic Burn-in, all inputs shall be connected through resistors to CP (Clock Pulse). Inputs that have pull up or pull down resistors may be connected to CP, VDD or Gnd. Outputs shall be open or connected through resistors to VDD. Bidirects shall be connected through resistors to VDD. R = 2.49K ohms ±10% resistor to reflect a 2mA minimum load condition.
2. CP = 100KHz ±15%; duty cycle = 50% ±15%; VIH = 2.5V to VDD; VIL = 0 ±.5V; transitions time < 0.5uS. An alternative (CP) or vector pattern may be applied to input pins depending on burn-in chamber limitations.
3. VDD(VCC) = Minimum, depending on oven capability, Maximum, depending on wafer process. (Typ: 3.6V – 8.0V) Limits and specifications also apply to any multiple voltage supplies.
4. I = input, O = output, T = three state output, PU = pull-up, PD = pull-down, B(I/O) = bidirect, N(M) = highest numbered inputs, bidirect, output, etc. as stated.

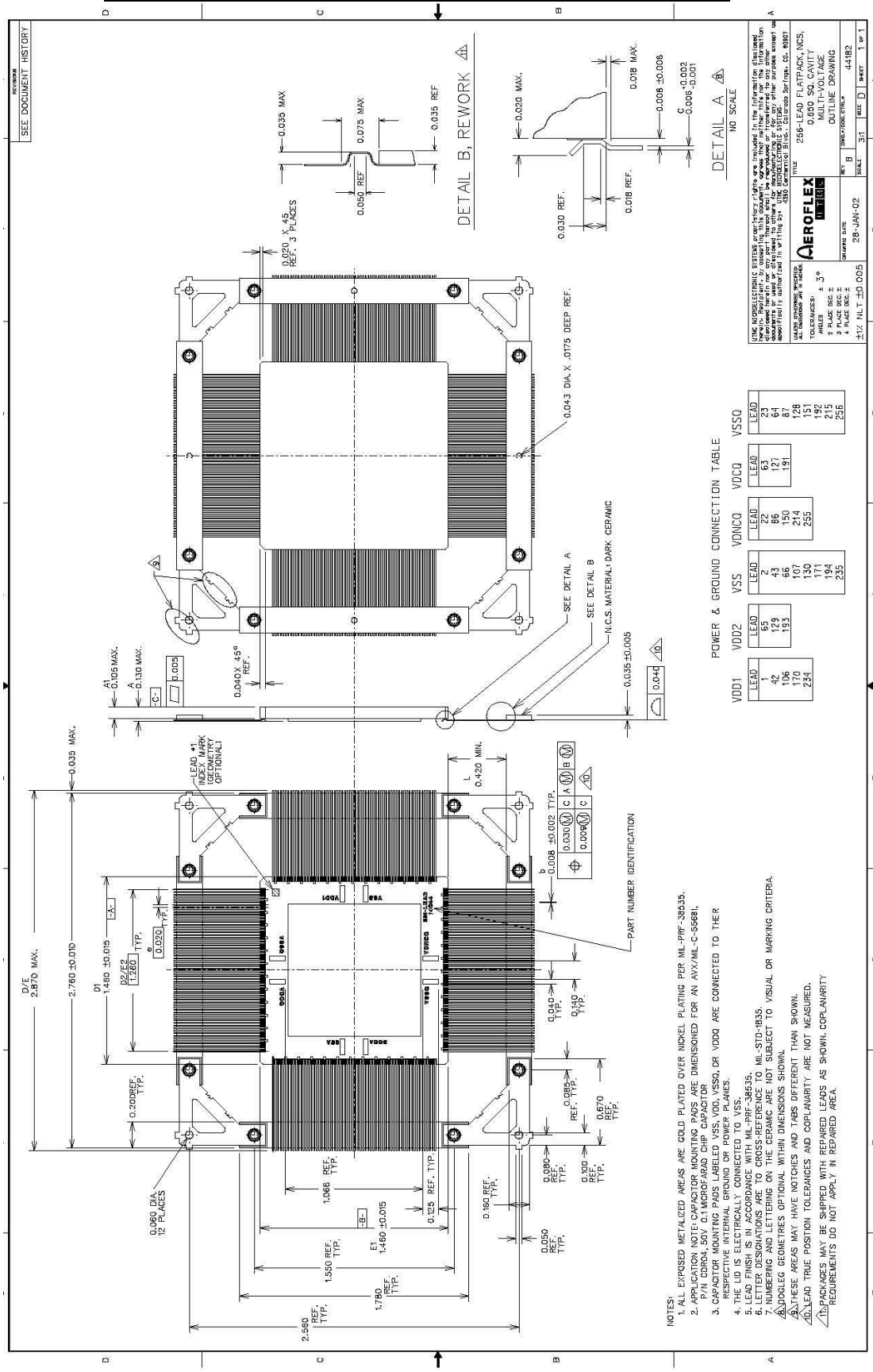



Figure 6: Package Outline Drawing – units in inches