BIT-PLANE ENCODER

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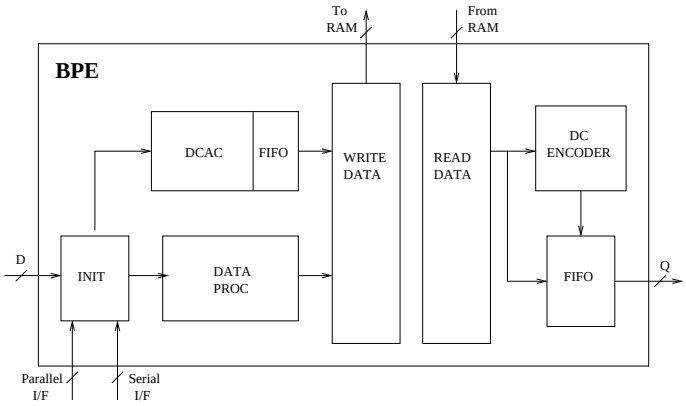
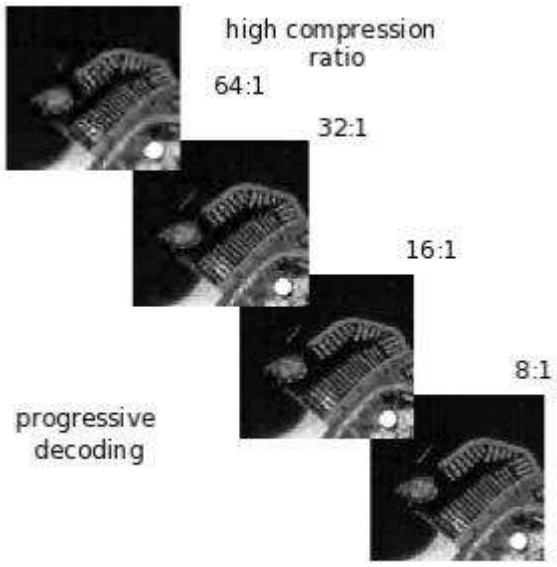
Features

- Full compliance with CCSDS 122.0-B-1[1]
- Lossy and lossless compression
- Progressive encoded data transmission
- Programmable bit-stream truncation and bit rate output
- Optimum, rather than heuristic, coding of quantized DC coefficients
- Programmable output headers
- Throughput: 20Msamples/s in 0.25um technology (20MHz @ 1 sample/clock)
- 24-bit, 2's complement, dynamic input sample range. Parallel 16-bit output.
- Stallable input and output data stream. Zig-zag and raster input order supported.
- Glueless interface to Aeroflex 3.3V Asynchronous Static RAM (or similar)
- Serial or parallel programming interface
- 3.3V IO, 2.5V core (typical core power for 16-bit image = 30mW/Msamples/s)
- TID tested to 50krad (Si) with potential value for over 100krad
- SEL immune to 120 LET
- Low SEU-induced bit error rate
- Flight parts packaged in Aeroflex 256-pin CQFP (44182)

Applications

- Executing CCSDS 122.0-B-1 *Image Data Compression* with DWT pre-processor module.
- Applicable to space frame-based image data with reconfigurable frame compression rate for deep-space and planetary missions.
- Applicable to push-broom and whisk-broom sensor data compression with *on-the-fly* compression rate reconfiguration for near Earth and planetary missions.
- Applicable to science data with more than two dimensions with excellent performance.
- Enabler for intelligent down-link rate control with fully embedded bit stream for progressive decoding.





1 *Image Data Compression*, Recommended Standard, CCSDS 122.0-B-1, Blue Book, November 2005

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1.0 Introduction

The Bit-Plane Encoder (BPE) is an ASIC which uses a sophisticated bit-plane encoding technique for compressing data output from a block transform such as the Discrete Wavelet Transform (DWT), Discrete Cosine Transform (DCT), or the Enhanced Discrete Cosine Transform (EDCT). In general, however, the BPE supports any decorrelator that produces 8x8 blocks of 24-bit 2's complement transform data where energy compaction tends toward the lower frequencies. The concatenated output bit string constitutes an embedded data format that allows progressive transmission and decoding since data transfer starts at a lower bits per pixel (bpp) rate and proceeds to a higher bpp rate. The BPE is highly customizable with over 40 parameters, many of which can be dynamically updated via two asynchronous interfaces. The BPE also supports numerous user-defined output headers and bit-stream truncation conditions.

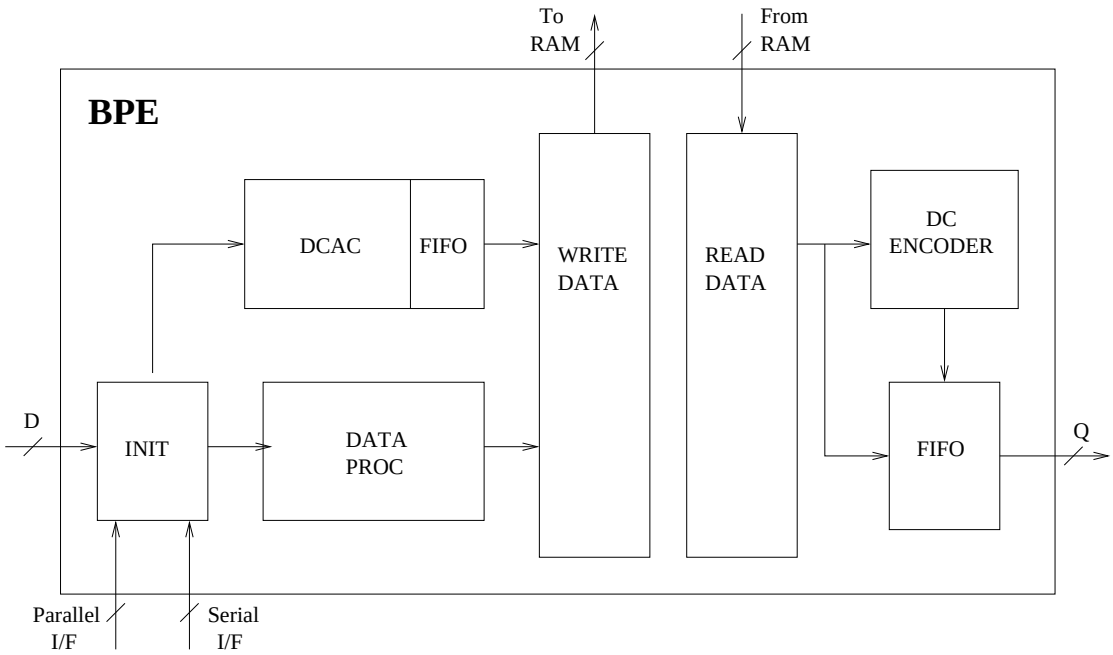


Figure 1-1: Bit-Plane Encoder (BPE)

2.0 Overview

Once initialized with the appropriate parameters via the parallel or serial interface, transform data in segment format is fed to the BPE via the D input bus (see Fig. 1-1). (A segment consists of a variable number of transform blocks and each transform block consists of one DC coefficient and 63 AC coefficients.) For each transform block, INIT separates the transform data, or coefficients, into DC and AC data. The INIT section determines the exact number of binary bits required to represent the maximum AC magnitude in each transform block. The latter value (hereafter termed "BitDepthAC_Block$_M$") and the DC coefficient are then sent to the DCAC section, while the 63 AC coefficients are sent to the DATA PROC section. The INIT section, according to certain parameters, also adjusts coefficients to allow for easier and more efficient coding. This includes reordering the AC coefficients and, when needed, applying user-defined weights to the input data.

The DATA PROC section is responsible for coding the 63 AC coefficients according to the CCSDS Image Data Compression Standard (reference [1]). DATA PROC examines the coefficients—starting from the highest bit-plane and progressing to the lowest bit-plane—and determines which data will be compressed. The compressible portions of the AC coefficient data are superficially mapped and coded to determine the most efficient coding scheme, per bit-plane, across several transform blocks. Once an efficient coding scheme is chosen, the coefficients are permanently mapped and coded according to this scheme and the data is concatenated and sent to the WRITE DATA section. Incompressible data is sent uncoded, but concatenated, to the WRITE DATA section.

The DCAC section collects DC coefficients and BitDepthAC_Block$_M$ values from the INIT section. To accommodate the progressive nature of the algorithm, the DC coefficients are grouped according to RAM width and parsed by bit-plane. The DC bit-planes are buffered, awaiting output to WRITE DATA along with the AC coded and uncoded data from DATA PROC. The BitDepthAC_Block$_M$ values are concatenated to reduce RAM size and also buffered for output to the WRITE DATA section.

The WRITE DATA section receives data from both DATA PROC and DCAC and writes that data to specific slots within the external RAM. The use of external RAM allows for the encoding of large segments as well as the averaging of data statistics across those segments. Normally, two external RAMs are necessary. As one RAM receives a segment's worth of transform blocks from WRITE DATA, the other RAM is providing a segment to READ DATA.

In the READ DATA section all data written by WRITE DATA is read from the RAM in a particular order, per reference [1]. The READ DATA section first reads DC bit-planes and sends them to the DC ENCODER section for compression, possibly leaving behind DC bit-planes that can be read out later in uncompressed form. The BitDepthAC_Block$_M$ values are read next and also sent to the DC ENCODER section. The latter data is followed by AC coded and uncoded data traversing from highest bit-plane to lowest bit-plane. The READ DATA section truncates reading according to user-defined ending conditions. For example, the user can stop data output for a segment immediately after the compressed DC coefficients have been output from the chip or truncate the bit-stream after a particular coded AC bit-plane has been encountered. AC data is sent to the output FIFO, where it's combined with the compressed DC coefficients and BitDepthAC_Block$_M$ values. Both READ DATA and WRITE DATA allow for several different RAM configurations.

The DC ENCODER section receives quantized DC coefficients and BitDepthAC_Block$_M$ values and compresses them according to reference [1]. In short, the first value received—either a DC coefficient or BitDepthAC_Block$_M$ value—serves as a reference and enters the bit-stream uncoded. Subsequent values are mapped and coded according to the differences they represent from the reference. The output of the DC ENCODER is a bit-stream of concatenated, coded values and ID bits, which are sent to the output FIFO.

The output FIFO buffers compressed data as necessary to support intermittent output data flows. The output bit-stream contains segment headers according to reference [1]. The 16-bit output is accompanied by a data ready signal as well as a few segment markers signals.

3.0 Operation

Operation of the BPE requires the connection of two external RAMs (see Fig. 3-1) and a suitable upstream decorrelator (not shown). Prior to use, the BPE must be reset and initialized with various parameters according to section 3.1. The initialization parameters, detailed in section 4, specify such things as external RAM selection, segment and image characteristics, header insertion, and bit-stream truncation conditions. Coefficient data is applied to the BPE via the D input bus and DVALID pin per section 3.4. Compressed data output can be expected on the Q output bus, accompanied by a high QRDY, according to section 3.6.

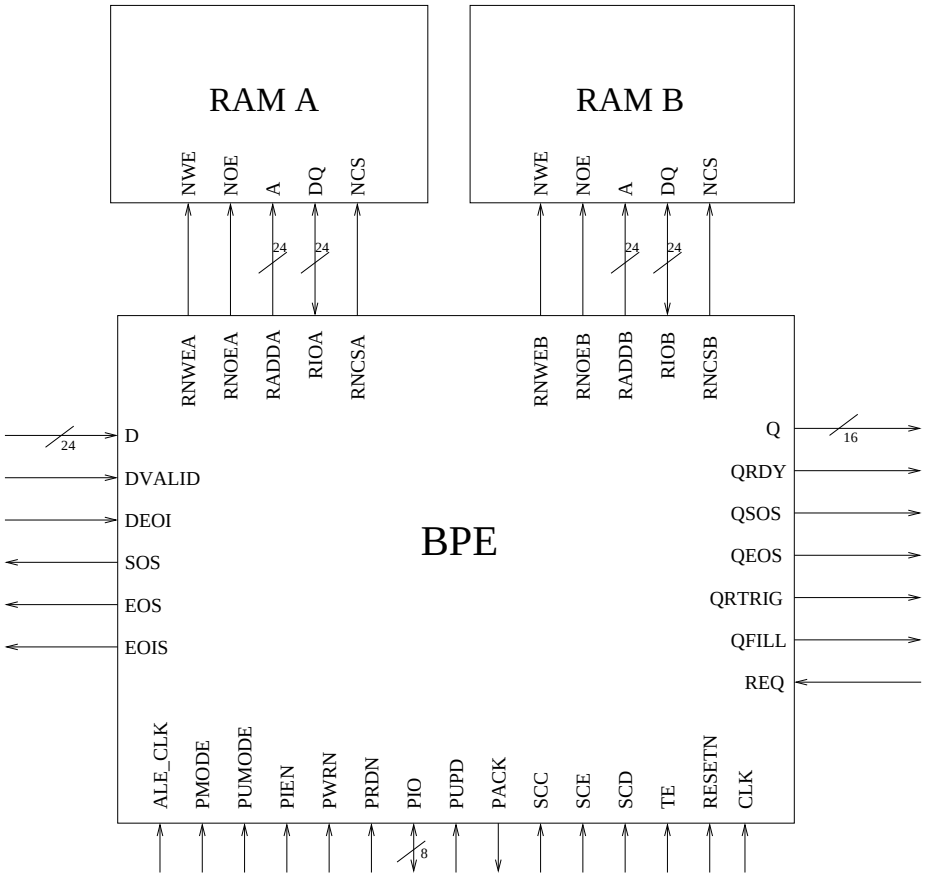


Figure 3-1: Bit-plane Encoder (BPE)[1]

[1] Pin assignments and descriptions are detailed in section 5.

3.1 BPE Initialization

The BPE must be reset using the RESETN pin and initialized with parameters via the parallel or serial interface. The first part of this process, detailed in section 6.5, is to activate RESETN for at least T_{RST} cycles of either CLK or SCC, whichever is slower. Immediately following reset, all BPE inputs must be in valid states. Once reset, the BPE must be passed initialization parameters via the parallel interface (or serial interface) using an 8051, FPGA, or similar host controller. The passing of parameters may begin T_{RSIE} (T_{RSEH}) cycles after RESETN is high. It is recommended that all parameters be initialized to appropriate values after a valid chip reset. Thereafter, any one or all parameters can be updated at the user's discretion provided they meet the requirements of section 3.2 (3.3). The host controller must wait T_{UHSS} (T_{ELSS}) cycles after the assertion of PUPD (or the passage of the 304th valid serial bit) before passing the first coefficient data to the BPE via the D[23:0] input bus.

3.2 Parallel Interface (PINT)

3.2.1 Overview

The BPE initialization parameters can be set using an 8-bit, bi-directional, parallel interface. The parameters are passed to the BPE using an external host controller such as an 8051 or FPGA (or similar). Although some parameters are meant to be permanent, all parameters can be set dynamically subject to the timing requirements of sections 6.6 and 6.8. The host controller can write parameters to the BPE, then read those same parameters from the BPE to verify a good transfer, as the parameters are stored in a RAM (PINT RAM) inside the BPE. The host controller can then signal an "update" (using the PUPD pin) to indicate that new parameters exist in the internal RAM and that those parameters should be used for any further data processing. The BPE will acknowledge this request, disable the interface, and eventually move the parameters from the RAM to the BPE internals, setting those parameters for the next data segment.

When updating a particular parameter it's important to note that most PINT RAM locations share parameters (see section 4.1). Take, for instance, PINT RAM address zero. The byte located at address zero is comprised of four parameters (and one unused bit). It is therefore not possible to update the HC parameter without, at the same time, updating (or writing) the EI, RES1, and HO parameters. If the user decides to update the HC parameter while keeping the values for the other three parameters the same, the new byte must be composed of the current EI, RES1, and HO values along with the new HC value.

Immediately following BPE chip reset, the PIO[7:0] bus must be driven (or connected to weak pull-ups or pull-downs) by the host controller regardless of the value of the PMODE pin. This bus must thereafter be driven at all times unless a PINT read is requested.

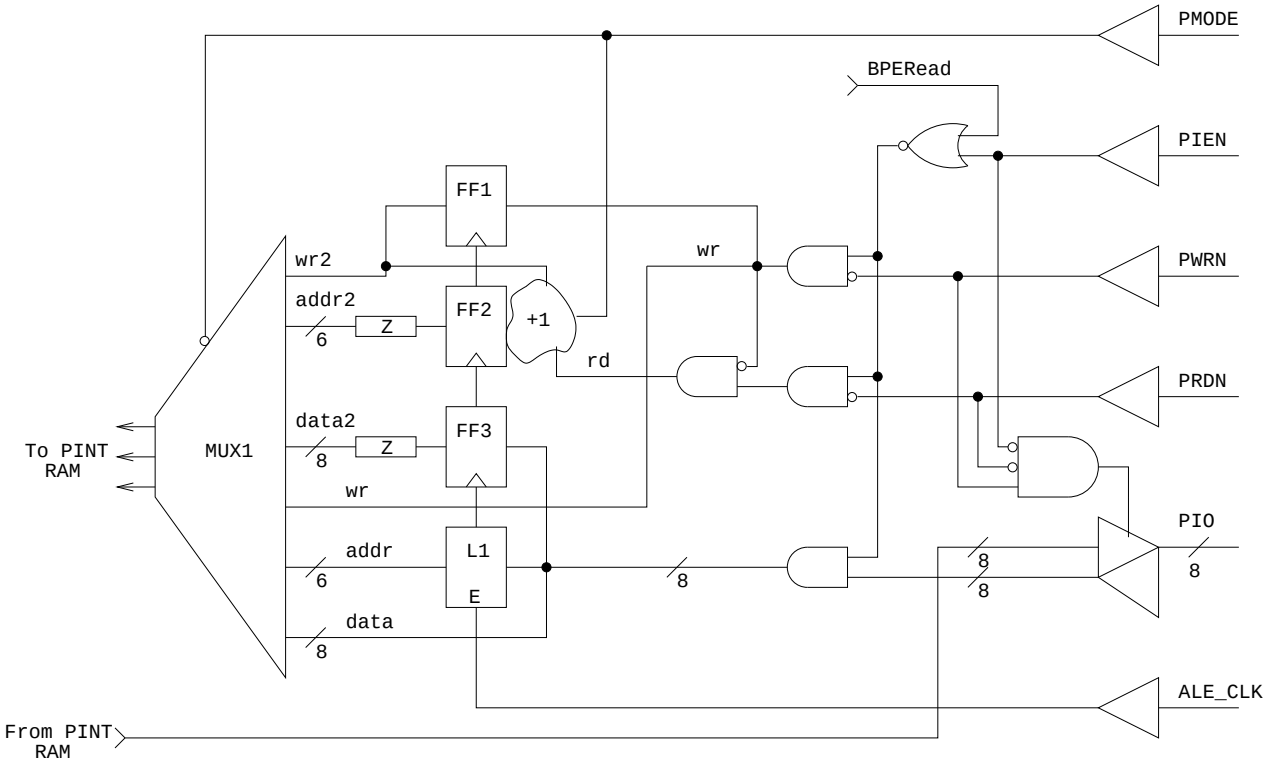


Figure 3-2: PINT Interface Diagram

The PINT uses a multiplexer, MUX1, to select between two sets of write signal, address, and data generation logic depending on the PMODE pin (see Fig. 3-2). When PMODE = 0, PINT RAM addresses (“addr”) result from latching the PI0[7:0] bus with L1 during a falling ALE_CLK. When PMODE = 1, PINT RAM addresses are created using a counter, FF2, which is incremented during a high “rd” or registered “wr” signal. In this mode, address (“addr2”) and data (“data2”) are delayed appropriately to avoid race conditions within the PINT RAM. In both modes, the write (“wr”) and read (“rd”) signals are high when PWRN and PRDN are low, respectively, and the PIEN is low. When the BPE is reading from the PINT RAM, the “BPERead” signal is high and all host controller writing and reading is disabled. The flip-flops FF1, FF2, and FF3, which are utilized when PMODE = 1, are asynchronously resettable. Therefore, the ALE_CLK pin does not have to be cycling during reset. The PUPD and PACK pins are not shown but are explained below.

3.2.2 Parallel Interface Modes

The parallel interface operates in two main operational modes depending on the host controller interacting with the BPE. The interface also utilizes two different parameter update modes. The various configurations of the BPE parallel interface are normally set by the host controller or hard-wired externally using pins PMODE and PUMODE.

The pin timing for these modes are detailed in 6.6.

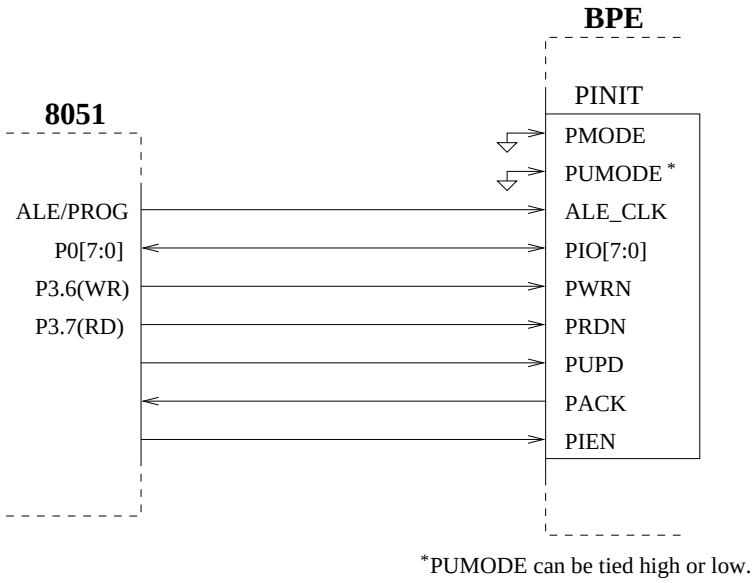


Figure 3-3: PINT Mode 0

PINT Mode 0 (see Fig. 3-3):

PINT Mode 0 (PMODE = 0) will allow address and data to be time-multiplexed on the BPE PIO bus according to the standard 8051 interface. This mode uses 8051 pins ALE/PROG, P0[7:0], P3.6(WR), and P3.7(RD) and connects them directly to ALE_CLK, PIO[7:0], PWRN, and PRDN of the BPE (other devices which might use the P0/PIO bus are not shown). The PIEN, PUPD, and PACK pins are connected at the user's discretion. The BPE PIEN pin must be asserted low by the 8051 to allow address and data transfer. Each byte transferred to or from the BPE via PIO[7:0] is associated with an address, starting from address zero. Since the internal RAM has a depth of 39 bytes, only the lower six bits ([5:0]) of the address are used, the upper bits being ignored. To force the BPE to use the new parameters for the next data segment, the 8051 should assert high the PUPD signal. See section 3.2.3 for PUPD handshake requirements.

This mode allows the most flexibility. Any and all parameters can be read or written by the 8051 at

any time. The 8051 can signal an update at its convenience, however the update must adhere to the restrictions of sections 6.6 and 6.8.

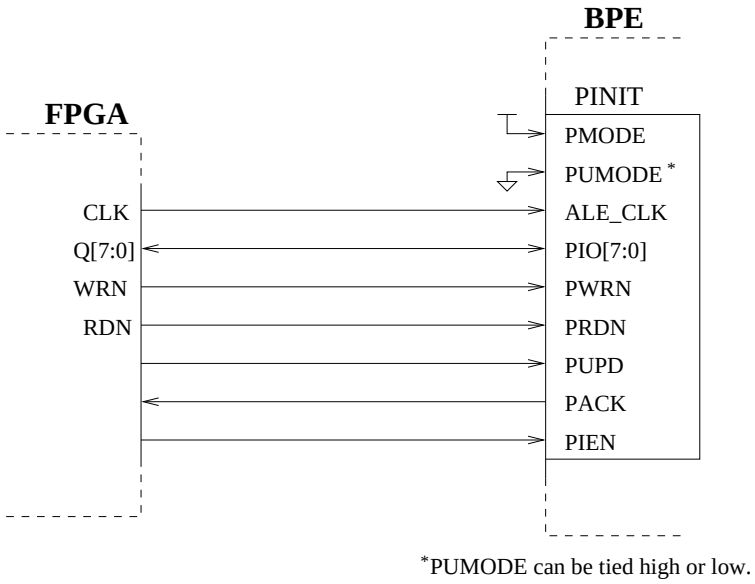


Figure 3-4: PINT Mode 1

PINT Mode 1 (see Fig. 3-4):

PINT Mode 1 (PMODE = 1) allows data-only transfers on the PIO bus synchronous to a clock input on the ALE_CLK pin of the BPE, such as can be achieved by an FPGA or equivalent device. The FPGA (or other device) uses BPE pins ALE_CLK, PIEN, PIO[7:0], PWRN, and PRDN to read/write data to the BPE. Similar to PINT Mode 0, the PIEN must be asserted low by the host controller to read or write. Bytes are passed sequentially, from address 0 to 38, on the rising edge of ALE_CLK. Since, in this mode, the BPE uses an internal address counter that is reset to zero, all 39 bytes must be passed to the BPE from the FPGA every time an update is desired. (Note that an extra, 40^{th} clock is necessary to force the internal counter to roll over.) For example, if the host controller wants to update only one parameter, it will have to write all 39 addresses, with only one parameter changed from the previous update. Also, the FPGA, in order to read one parameter, must read all 39 addresses. Writing or reading all 39 addresses ensures the BPE's internal address counter is synchronized with the data. Once new parameters have been written to the BPE, the FPGA can signal an update, subject to the PUPD handshake constraints mentioned in section 3.2.3.

This mode, though not as flexible as PINT Mode 0, allows the BPE to interface to the regular data port of any device, FPGA or otherwise.

3.2.3 Parameter Update Handshaking

Once there are valid parameters in the PINT RAM, the host controller can assert high the PUPD pin. This assertion can be delayed as long as desired, but can occur no earlier than one host controller clock cycle after the last byte transfer. In order to set parameters for the next segment, the assertion must occur T_{UHSS} cycles before the start of the next segment per sections 4.5 and 6.8. Note that PIEN does not have to be low for a PUPD assertion.

Once the PUPD pin is brought high, it must be held high until the the PACK signal is asserted high; this is the well-known "handshake" for crossing clock domains. The handshake can be held as long as desired, but note that the PACK signal will not drop low until the PUPD signal drops low. Reading or writing parameters during the handshake is not recommended. Typically, the PUPD signal should be asserted low as soon as the host controller senses an active PACK signal. PACK pin operation is detailed in section 3.2.4.

3.2.4 Update Acknowledge Modes

PACK signal response depends on the condition of pin PUMODE.

Acknowledge Mode 1 (PUMODE = 1):

In Acknowledge Mode 1, the PACK pin will be asserted high once the PUPD signal has been sensed active high internally by the BPE. This mode provides a quick acknowledge to an PUPD signal, minimizing the pin-polling time of the host controller.

Acknowledge Mode 0 (PUMODE = 0):

In Acknowledge Mode 0, the PACK pin will be asserted high once the PUPD signal has been sensed active high internally by the BPE *and* all parameters have been passed from the PINT RAM to the BPE internals. This mode indicates to the host controller when parameters have truly been passed to the BPE internals and when the interface has been re-enabled.

3.3 Serial Interface (SINT)

The BPE may also receive initialization parameters via the SINT. After reset, to use the SINT, the user must run the SCC, bring SCE high, and use the SCD pin to set the first data bit (hereafter called “the enable bit”) to one. SCE high and SCD high will enable the interface. Every SCD bit *after* the first bit will be clocked into the SINT provided SCE is high and SCC is running (for timing requirements see section 6.7). As the user clocks in data, the SINT uses a counter to determine when the internal serial register is full (the order of the parameters is per section 4.2). The serial register is considered full when SCD has been valid for 303 SCC clock cycles (not including the enable bit). Once full, the interface will be disabled and any further clocking/enabling will have no effect. Handshaking is not necessary since parameters from the SINT are automatically transferred to the BPE internals once the serial register is full. To re-initialize the SINT for use with other segments of data, the user must bring SCE low while SCC is running. To clock in another set of data, the user must again bring the SCE and SCD pins high. However, the user must wait a minimum of $5T_{SCCW}$ before re-enabling the interface to allow time for the BPE to recognize that new parameters exist.

The SINT input bit-stream is stallable provided the timing requirements of section 6.7 are met and the input stream is not stalled across segment boundaries, as this has ill effects. Further, SCE, SCD, and SCC must always be at valid logic levels. Similar to the PINT, there exists a “parameter preclusion period” during which the serial interface cannot be operating (see sections 4.5 and 6.8). Assuming there are no input wait states (DVALID = 0), serial data transfer must begin after the SOS pin is brought low and completed before the EOS pin is brought high.

3.4 Coefficient Data Input

The BPE accepts any transform coefficient data which, when parsed, can be represented by a series of 8x8 blocks. For best compression, however, the lowest frequency coefficients must heavily influence the upper-left corner of each block (see reference [1]). The coefficients must be in 2's complement format and fed to the D[23:0] input bus accompanied by an active DVALID signal per the timing requirements of section 6.10. Data on the D[23:0] bus is interpreted as right-shifted, that is, D[0] represents the LSB of the input coefficient. All coefficient bits above D[NB – 1], where “NB” is the parameter NB, are ignored. (Ignored coefficient bits must still be at valid logic levels.) Input data is segmented according to the S parameter, where S indicates the number of 8x8 transform blocks in a segment. Continuous data input is not necessary since, on segment boundaries, the BPE automatically processes and drains its internal pipeline structure, as long as REQ is high.

Although the BPE accepts coefficient quantizations of 24 bits, the low frequency, or DC component, processing of the BPE accepts only 21 bits. Therefore, the parameter WDC must be set according to Eqn. 3.4.1 when the DC coefficient width, represented by the parameter NB, is greater than 21 bits.

$$WDC = NB - 21 \qquad (3.4.1)$$

The order of the coefficients entering the BPE is important. The BPE supports two types of coefficient ordering: raster and zig-zag. The order in which the BPE interprets input data is set by the ZIG parameter (see section 4.3). In all cases, the first coefficient in a transform block must be the lowest frequency component; the last coefficient must be the highest frequency component. If the image data entering the BPE is transposed, this must be noted using the TPOSE parameter. Although the upstream chip may transpose its image, this has no effect on BPE compression other than to change the TPOSE bit set in the BPE headers (see reference [1]). Tables 3-1 and 3-2 detail the input ordering scheme for blocks within the segmented data and are intended to be viewed as a 1-to-1 correlation with Fig. 4-1 of reference [1].

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

Table 3-1: Parameter ZIG = 0.

1	2	6	7	15	16	28	29
3	5	8	14	17	27	30	43
4	9	13	18	26	31	42	44
10	12	19	25	32	41	45	54
11	20	24	33	40	46	53	55
21	23	34	39	47	52	56	61
22	35	38	48	51	57	60	62
36	37	49	50	58	59	63	64

Table 3-2: Parameter ZIG = 1

The BPE allows for varying segment sizes provided that these changes occur on segment boundaries and the S parameter is updated accordingly. Yet, due to the pipeline nature of the BPE, there are some constraints on segment size variation:

$$\text{OutputWordCount}_{\text{Segment1}} + T_{WAIT1} + 64 = \text{InputWordCount}_{\text{Segment2}} + T_{WAIT2} \qquad (3.4.2)$$

where "$\text{OutputWordCount}_{\text{Segment1}}$" is the number of compressed output words for the segment currently being output, and
"$\text{InputWordCount}_{\text{Segment2}}$" is the number of input coefficients for a segment that follows segment 1, and
"T_{WAIT1}" is the number of CLK cycles during which the REQ pin is low while segment 1 is output, and
"T_{WAIT2}" is the number of CLK cycles during which DVALID is low while segment 2 is input.

This constraint is particularly important when a large segment is followed by a much smaller segment. Each of the two external RAMs (see Fig. 3-1) accessed by the BPE support only one segment at a time. So, while one RAM is outputting a segment, the other is receiving a segment. While the larger segment (segment 1) is still being output from one RAM, the smaller segment (segment 2), meanwhile, has already been written to the other RAM. If the upstream chip were to send segment 3 while segment 1 is still being output, segment 2 would be over-written. To avoid this, the user must insert wait states (DVALID = 0), the sum of which is equal to T_{WAIT2} CLK cycles. Since the problem occurs during segment 3, the wait states can be inserted anytime before, during, or after the application of segment 2. It's important to remember that $OutputWordCount_{Segment1}$ is not only a function of image statistics but also of bit-stream truncation conditions (see section 3.6.2).

It is not necessary to establish image boundaries as the BPE can process segment data indefinitely. Yet, if desired, the user can signal to the BPE that an end-of-image is forthcoming via three methods. First, the DEOI can be pulsed or held high, synchronous to CLK, during the last segment in an image. Second, the parameter EI can be set to one via the PINT or SINT, indicating that the *current* segment is the last segment in an image. Both the DEOI pin and the EI parameter are not recognized after a segment has ended. The latter pin and parameter are recognized only during the application of segment data, although DVALID does not have to be high. Third, if the DEOI pin or EI parameter is not going to be used, the IGSEG and ISEG parameters can be used, both of which are set via the PINT or SINT. Per section 4.3, IGSEG can be cleared (set to zero) and the ISEG parameter set to the number of segments in an image. The BPE will then automatically establish image boundaries. The notion of images has no effect on compression, but does affect BPE header 1A and 1B generation (see reference [1]).

3.5 External RAM Interface

The BPE normally requires two external RAMs (see Fig. 3-1). The BPE supports RAM word depths from 2k to 16M according to the parameter RAM[3:0]. RAM word width is either 16 or 24 bits (set by parameter R16) and is representative of the maximum quantization at the D[23:0] input bus. For instance, if the quantization is less than 15 bits, then R16 may be set to one, otherwise R16 must be zero. If RAM width is chosen to be 24 bits (R16 = 0) when only 16 bits are necessary, only the 16 LSBs of the RIOA(B)[23:0] bus will be used. In the latter case, the RAM can hold more pixels than if R16 was set (see Table 4-3).

The RAMs are “ping-ponged” as necessary to support a continuous data flow. For example, after initialization RAM A will receive the first segment of data. Once RAM A receives all of the first segment, RAM A will immediately output that segment. Meanwhile, RAM B will receive the second segment, if one is available. Once RAM A completes the outputting of the first segment, RAM A will be set to receive the third segment while, at the same time, RAM B outputs the second segment. If data segments are sent to the BPE on an infrequent basis, it's possible to operate the BPE using RAM A only (see below).

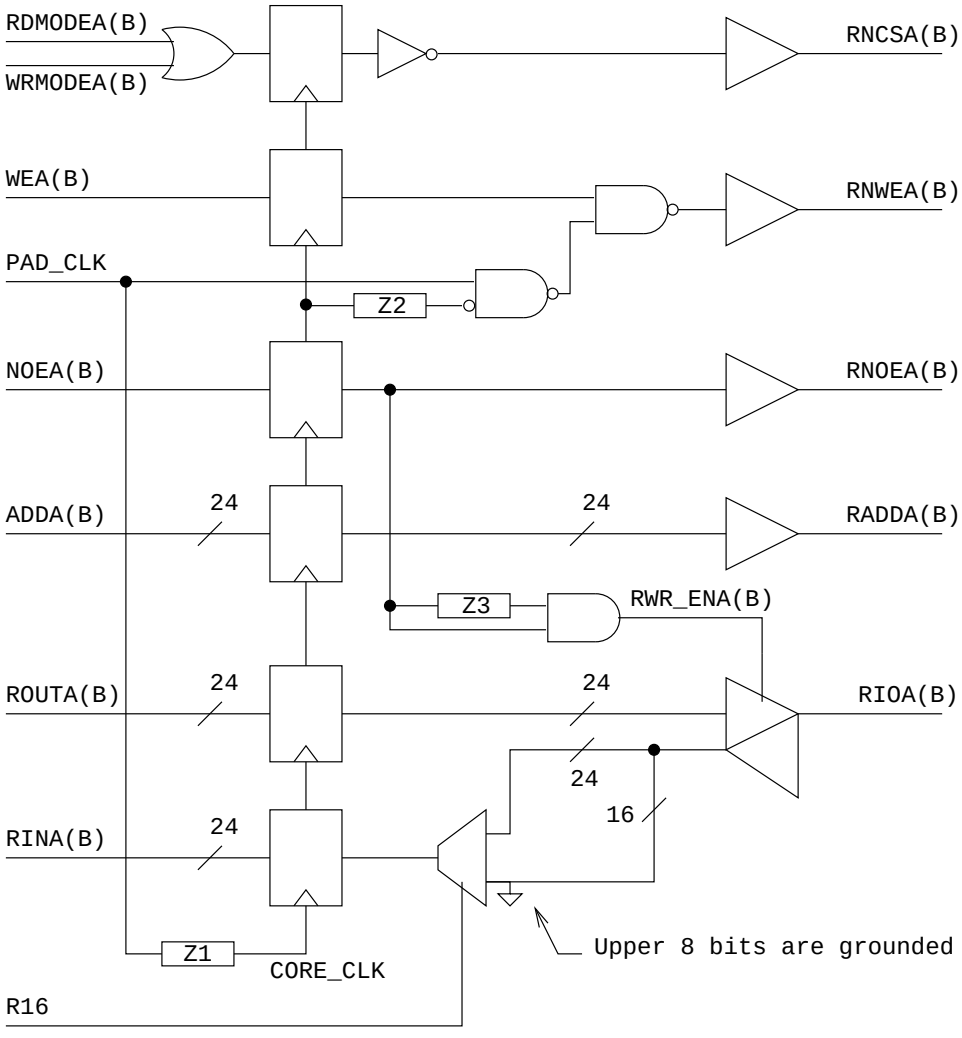


Figure 3-5: BPE RAM Interface

The BPE's internal RAM interface is shown in Fig. 3-5. The BPE is designed to interface to 3.3V Asynchronous Static RAMs, such as the HX6256, HX6408 or similar SRAMs from other manufacturers (see timing diagrams in 6.11). Immediately after BPE chip reset, RNCSA(B), RNOEA(B), and RNWEA(B) will be set high, and the BPE will drive both RAM RIOA(B) buses. RNCSA(B) will be active low whenever a RAM is in write mode (WRMODEA(B) = 1) or read mode (RDMODEA(B) = 1). When a RAM is neither writing nor reading, RNCSA(B) will be high and the RAM can be set to a low power or standby mode.

While in write mode, a RAM will receive segment data from the BPE, and the RAM's DQ bus output drivers will be in a tri-state condition since RNOEA(B) will always be high. In this mode, the BPE will always drive the RIOA(B) bus and will never tri-state that bus. The address and data bus are driven through staggered delays (not shown) to minimize the instantaneous current drawn by the pads.

The RNWEA(B) signal is generated using two clocks, one skewed slightly from the other. PAD_CLK is the signal which comes directly from the BPE input clock pad. CORE_CLK is the delayed version of the PAD_CLK which drives all of the BPE's core flip-flops. Z1 represents the amount of delay between PAD_CLK and CORE_CLK. What results is a shortened RNWEA(B) pulse which is high for T_{WHWL} (see Fig. 6-12). Address and data setup times (T_{CHWL} - T_{CHDV}) are satisfied since, due to the delay Z2, RNWEA(B) is slow to activate when compared to address and data. Address and data hold times (T_{CHDV} - T_{CHWH}) are preserved since the interface flip-flops are driven by the slower CORE_CLK while RNWEA(B) activation is quickly curtailed by a high PAD_CLK.

In read mode, a RAM will continuously output data and therefore always drive the RIOA(B) bus while the BPE's output drivers are in a tri-state condition. The continuous outputting of data eliminates RIOA(B) bus contention problems, except when switching a RAM from writing to reading or vice-versa. RIOA(B) bus contention during switching is minimized since the RWR_ENA(B) signal is designed to be slow to rise, due to delay Z3, but quick to fall. As a result, the BPE is slow to take control of the RIOA(B) bus, but, when necessary, will quickly relinquish control to the RAM. This might create short periods during which the RIOA(B) bus will be floating and not driven. To avoid this, weak pull-ups (or pull-downs) can be connected to the RIOA(B)[23:0] bus.

An unusual system configuration is possible when data segments occur so infrequently that the BPE can process and output a segment before another segment is input. In this case, only one external RAM is needed. If this mode of operation is desired, the parameter RAMA must be set. To operate in this mode, the user must input a segment of data using the D[23:0] bus and simply wait for a valid QEOS before inputting another segment.

3.6 Compressed Data Output

When output data is available, the QRDY pin is asserted high. The QRDY pin will remain high while valid, left-justified data is on the Q[15:0] output bus. A valid data transfer occurs when QRDY is high and the REQ pin is active high per the timing requirements of section 6.10.

The REQ pin throttles the compressed output data flow, and because the data within the BPE is pipelined, this pin has a few timing requirements. The amount of time during which the REQ pin must be high depends upon the nature of the coefficient data applied to the BPE. Using two external RAMs, the BPE is capable of safely managing two full segments. As a result, it is acceptable to send two segments to the BPE even while REQ is held low either during or after the segment transfers. However, compression data corruption will occur if, while two segments are stored in the external RAMs and the REQ pin is forced low, a third segment is started at the input of BPE. If the BPE is continuously receiving data for multiple segments—not merely accepting coefficient data for one particular segment—then the REQ pin must be high roughly 20% of the time to avoid data corruption. For example, if the total compressed word count for three outgoing segments is 500k words, and therefore requires 500k valid output transfers, then REQ must be high for at least 400k of those transfers. If the downstream chip is always accepting data, it's possible to tie the REQ pin high.

Data output is accompanied by several segment markers which are only asserted during a valid data transfer. QSOS and QEOS are high during the first and last output word in a segment, respectively. QFILL is asserted high when the FILL parameter is set and the output word consists only of fill bits (zeros). QRTRIG is pulsed when the number of output words equals the parameter ROUT.

Chip output latency (T_{QLAT} of section 6.10) depends on image statistics, segment size, parameters JA and JU, and pipeline delays, the variations of which normally total less than 1024 CLK cycles. Assuming coefficient data is continuously supplied and output data is continuously read, the BPE chip latency is thus:

$$S * 64 < T_{LAT} < 1024 + S * 64 \qquad (3.6.1)$$

where “S” is the parameter S of section 4 (Table 4-2) and reference [1].

3.6.1 Compressed Data Output Headers

Header 1A and, possibly, 1B of reference [1] automatically precede all compressed data output in a segment. Additional headers described in reference [1] as well as an extra, non-CCSDS compliant header (header 5) can be programmed for output using the parameters described in detail in section 4.3. Specifically, the header configuration parameters HC[3:0], HSTART[3:0], HPER[3:0], and HTYP[3:0], when applicable, designate which headers will be inserted:

Header Configuration Bit	***Header***
3	5[1]
2	4
1	3
0	2

[1] Header 5 is not part of reference [1].

For example, if HSTART[3:0] = '1011' then headers 5, 3, and 2 will be inserted into the BPE output bit-stream at the appropriate time specified in section 4.3. If a header configuration parameter (e.g. HSTART[3:0]) is set to all zeros, this implies that only header 1A and, possibly, 1B will be inserted. If it's desired that every header be identical, the user need only set all header configuration parameters to the same value.

Header 5 consists of the BPE mappings: MAP4[63:0], MAP3[23:0], MAP2[7:0]. Therefore, the MSB of MAP4 and the LSB of MAP2 form the first occurring bit and the last occurring bit, respectively, in header 5. If header 5 is used, its presence may be signaled by the first reserved bit in header 1A. Note, however, that this would not conform to the CCSDS standard in reference [1].

The BPE hard-codes several header bits. In header 3, both “OptDCSelect” and “OptACSelect” are permanently set to one. In header 4, “CodeWordLength” is set to “01.”

To prevent conflicts, certain header configuration parameters have priority:

Header Configuration Parameter	***Priority***
HC[3:0]	1
HSTART[3:0]	2
HPER[3:0]	3
HTYP[3:0]	4

In all cases, when HO is set high, the headers specified by HC[3:0] override all other header configuration parameters. If HO is set low and HSTART[3:0] is due for insertion, HSTART[3:0] overrides HPER[3:0] and HTYP[3:0]. Likewise, if HPER[3:0] is due for insertion, it will only override HTYP[3:0]. HTYP[3:0] has the lowest priority.

3.6.2 Compressed Data Output Truncation

The compressed output bit-stream is truncated according to the parameters ROUT[23:0], BPST[4:0], STGST[1:0], DCST, APPROX, and FILL. The numerous truncation conditions that result from these parameters are herein divided into truncation modes (see Table 3-3). Note that, if desired, these modes can be changed every segment via the PINT or SINT.

Truncation Mode	***Description***	***Parameters***					
		ROUT[1]	***BPST***	***STGST***	***DCST***	***APPROX***	***FILL***
Lossless	Output entire compressed segment	$[0..2^{24} - 1]$	0	3	0	0	{0,1}
Fixed Rate	Output exactly ROUT words	$[0..2^{24} - 1]$	0	3	0	0	1
Approximate Rate[2]	Output ROUT words, approximately	$[0..2^{24} - 1]$	n/a	[0..3]	{0,1}	1	{0,1}
Quality	Output to specified bit-plane quality	$[0..2^{24} - 1]$	[0..23]	[0..3]	0	0	{0,1}
Thumbnail[2]	Output thumbnail quality	$[0..2^{24} - 1]$	n/a	n/a	1	0	{0,1}

Table 3-3: Output Truncation Modes

[1] First, note that ROUT is a modulo 2^{24} number. Second, note that, depending on the truncation mode, ROUT must be set to a value greater than or equal to the number of compressed output words (not bytes) required to meet the desired condition or quality. For example, if an output segment consists of 1000 compressed words, and the lossless truncation mode is desired, ROUT must be set greater than or equal to 1000.

[2] BPST and STGST parameters, although not applicable, must be set to some valid value.

In general, coded output data stops at the BPST and STGST location or when the number of output words equals ROUT, whichever occurs first. If FILL is set, the BPE will fill with zeros until the ROUT condition is satisfied.

In all truncation modes, regardless of ROUT:

1. if a segment lacks coded data, headers will be output at the minimum (per 3.6.1).
2. if a segment has coded data, then headers and DC data per sections 4.3.2 and 4.3.3 of reference [1] will be output at the minimum.

When in Approximate Rate mode, the BPE will output data until the ROUT condition is satisfied, regardless of BPST. Once ROUT is met, the BPE will continue to output data until the output stage specified by STGST or DCST (DCST has priority over STGST) has completed. If the desired stage for the current bit-plane has already been output, the bit-stream will stop once the current stage is completed.

For further details on output bit-stream truncation, see section 4.2.3.2 of reference [1] and examples in reference [2].

4.0 Initialization Parameters

4.1 Parallel Interface (PINT) Parameter Locations

PINT Address	***Parameters MSB(7)->LSB(0)***	***PINT Address***	***Parameters MSB(7)->LSB(0)***
0	**0**, EI, RES1[5], HO, HC[3:0]	20	ISEG[7:0]
1	ROUT[23:16]	21	UMAP, NTYPE[1:0], NB[4:0]
2	ROUT[15:8]	22	R16, RAMA, ZIG, 0, RAM[3:0]
3	ROUT[7:0]	23	JA[1:0], JU[1:0], TEST[3:0]
4	DCST, BPST[4:0], STGST[1:0]	24	WDC[1:0], WP0[1:0], WP1[1:0], WP2[1:0]
5	FILL, APPROX, **0**, **0**, RES2[3:0]	25	WC0[1:0], WC1[1:0], WC2[1:0], WG0[1:0]
6	S[19:12]	26	WG1[1:0], WG2[1:0], **0**, **0**, **0**, **0**
7	S[11:4]	27	MAP4[63:56]
8	S[3:0], **0**, **0**, RES3[1:0]	28	MAP4[55:48]
9	PADROW[2:0], RES1[4:0]	29	MAP4[47:40]
10	DWT, RES4[13:12], SIGN, N[3:0]	30	MAP4[39:32]
11	WID[19:12]	31	MAP4[31:24]
12	WID[11:4]	32	MAP4[23:16]
13	WID[3:0], TPOSE, RES4[11], UWTS, RES4[10]	33	MAP4[15:8]
14	RES4[9:2]	34	MAP4[7:0]
15	RES4[1:0], IGSEG, HPERS, HPER[3:0]	35	MAP3[23:16]
16	HPERCNT[15:8]	36	MAP3[15:8]
17	HPERCNT[7:0]	37	MAP3[7:0]
18	HSTART[3:0], HTYP[3:0]	38	MAP2[7:0]
19	ISEG[15:8]		

Table 4-1: Parameter Locations Within PINT

The 8-bit parameter data at a given PINT address is shown in descending order, from MSB to LSB. For example, the EI parameter at address zero is located at bit position 6 and is written to the PINT using pin PIO[6]. Note that there are ten unused bits (annotated as '**0**' or '0' in Table 4-1). These bits must always be cleared, or written, as 0.

4.2 Serial Interface Parameter Order

The order of serial data is identical to the parallel interface order specified in Table 4-1, except that nine unused bits ('**0**') are not included in the bit-stream. Please note that address 22 contains a '0' which must be included in the serial bit-stream. When the serial interface is used, the first bit input should be '1' (which enables the interface). After that the parameter order is EI, RES1[5], HO, HC[3], HC[2] ... MAP2[1], MAP2[0]. See section 3.3 for serial interface operation.

4.3 Parameter Description

With the exception of weights and mappings, all parameters must be initialized to appropriate values prior to sending the first coefficient data to the BPE, especially when using PINT Mode 0 (see section 3.2.2). The latter requirement is a moot point when using PINT Mode 1 or the serial interface since, in those modes, it is necessary to write all parameter bits. Contingent upon proper parameter passing per sections 6.5 and 6.8, most parameters that are written during a certain segment (or image) are applied during the following segment (or image). Those parameters properly applied to the BPE remain in effect until changed via one of the two interfaces, except for EI and HO.

The parameters in Table 4-2 are described in detail in reference [1] and therefore will not be explained here:

BPE Parameter	***Equivalent CCSDS Parameter***	***BPE Parameter***	***Equivalent CCSDS Parameter***
ROUT[23:0][1]	SegByteLimit	WP0[1:0]	CustomWtHL3
DCST	DCStop	WP1[1:0]	CustomWtLH3
BPST[4:0]	BitPlaneStop	WP2[1:0]	CustomWtHH3
STGST[1:0]	StageStop	WC0[1:0]	CustomWtHL2
FILL	UseFill	WC1[1:0]	CustomWtLH2
S[19:0]	S	WC2[1:0]	CustomWtHH2
PADROW[2:0]	PadRows	WG0[1:0]	CustomWtHL1
DWT	DWTType	WG1[1:0]	CustomWtLH1
SIGN	SignedPixels	WG2[1:0]	CustomWtHH1
N[3:0]	PixelBitDepth	RES1[5:0][2]	Header 1 Reserved Bits
WID[19:0]	ImageWidth	RES2[3:0][2]	Header 2 Reserved Bits
TPOSE	TransposeImg	RES3[1:0][2]	Header 3 Reserved Bits
UWTS	CustomWtFlag	RES4[13:0][2]	Header 4 Reserved Bits
WDC[1:0]	CustomWtLL3		

Table 4-2: CCSDS Parameters Name Matching

[1] The BPE only supports modulo 2^{24} for ROUT (SegByteLimit), as opposed to reference [1]. Note also that ROUT = SegByteLimit / 2.

[2] The bit order of the reserved bits directly corresponds to that specified in reference [1].

With the exception of the header configuration parameters and mappings, all parameters below, which are not part of reference [1], are unsigned binary integers.

EI—End Image

When set high (set to one), indicates that the *current* segment is the last in an image. This functionality is different from all other parameters since its assertion takes effect during the *current* segment. EI is ignored thereafter until either the SINT is used for a parameter update or an update occurs to *any* PINT address. This means that if EI is set during a parameter update, it will end the current image but will afterwards have no effect. If no further parameter updates occur, EI will remain set, but will have no effect on image truncation. If EI is set during a parameter update, it must be cleared during any subsequent parameter updates if it's desired to continue processing the same image. The EI parameter cannot be used to end an image "outside" of the SOS and EOS segment marker signals. (For SOS and EOS timing see section 6.9). That is, the EI parameter is ignored once a segment has ended, but will be re-sampled once another segment has begun and a parameter update has been performed. Do not confuse this parameter with the DEOI input pin that can also be used to end an image during the same segment in which it is asserted.

IGSEG—Ignore Image Segment Count

When set high, it means that an image will be ended by the EI parameter or the DEOI pin, rather than the on-chip segment counter. When cleared, indicates that an image will be ended after ISEG number of segments. The user may change this parameter anytime during an image, but it will not take effect until the start of the next image (see section 4.5)

ISEG[15:0]—Image Segment Count

Depending on IGSEG, this parameter specifies the number of segments in an image, modulo 2^{16}. (The term “modulo 2^{16}” implies that setting ISEG = 0 is equivalent to setting ISEG = 2^{16}.) The user may change this parameter anytime during an image, but it will not take effect until the start of the next image.

EI and DEOI will always end an image regardless of IGSEG and ISEG. Although, if DEOI is activated or the EI parameter is set, the ISEG internal counter will reset.

The following example shows how ISEG can be used to determine the number of segments in an image. The division of data into images has no effect on compression, but does change the BPE output headers per reference [1].

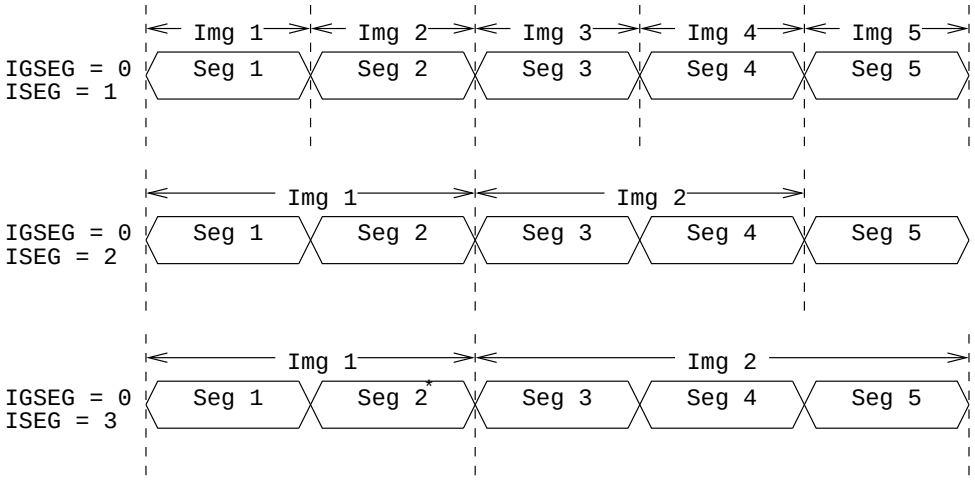


Figure 4-1: IGSEG and ISEG Example

HO—Header Override

The functionality of HO is similar to EI. However, when set high, this parameter indicates that the header configuration for the *next* segment will be that specified by the HC parameter. HO is ignored thereafter until either the SINT is used for a parameter update or an update occurs to *any* PINT address. This means that if HO is set during a parameter update, the header specified by HC is inserted only once. If no further parameter updates occur, HO will remain set, but will have no effect on the BPE output headers. If HO is set during a parameter update, it must be cleared during any subsequent parameter updates if it's desired to not use HC to specify BPE headers.

HC[3:0]—Header Override Configuration

When HO is set high, this parameter specifies the header configuration regardless of HSTART, HPER, or HTYP. As stated in the HO parameter description, HC will only take effect once per parameter update, when HO is set high.

HSTART[3:0]—Header Start

After the BPE is reset, this header configuration specifies the output headers for the *first* segment only —assuming HO is not set—regardless of HPER, and HTYP.

HPERS—Header Periodic Segment

When set low, HPERS indicates that the periodic header configuration, specified by parameter HPER, is to be inserted at the beginning of every HPERCNT images. That is, HPER insertion is based on counting images. In this case, an HPERCNT = 1 forces HPER header insertion every image. When set high, it indicates that HPER headers are inserted at the beginning of every image and, within each image, every HPERCNT segments. That is, HPER insertion is based on counting segments. If HPERCNT = 1 and HPERS = 1, then the header configuration (HPER) will be inserted at the beginning of every segment. See Fig. 4-2 and Fig. 4-3.

If the user changes HPERS, then the internal counter associated with counting segments or images is reset. Insertion of the next HPER header depends on the final state of the HPERS parameter. For example, consider a scenario when HPERS = 0. This specifies the HPER header is inserted every HPERCNT images. If during an image HPERS is set to a 1, then the internal counter is reset and the HPER header will be inserted in the data stream at the beginning of the next segment. Thereafter, HPER will be based on segments and inserted every HPERCNT segments and at the start of an image. If the opposite occurs, with HPERS = 1 changing to HPERS = 0 within a sequence of segments, the internal counter is reset; the next HPER header will occur in the segment starting the next image. That insertion is the first image count and after a total of HPERCNT images another HPER header configuration is output.

HPER[3:0]—Header Periodic

Depending on HPERS and HPERCNT, this header configuration is used to specify the output headers. HC (when HO is set high) and HSTART override HPER.

The following example shows how often the header—specified by HPER[3:0]—is inserted when HPERS = 0 with various HPERCNT[15:0] values. Note that the data is divided into images, not segments, and, because of this, HTYP header insertions are not shown. Normally, HPER would first be inserted at the beginning of image 1 (“Img 1”). However, since the beginning of image 1 corresponds to the first segment after reset, HSTART overrides HPER.

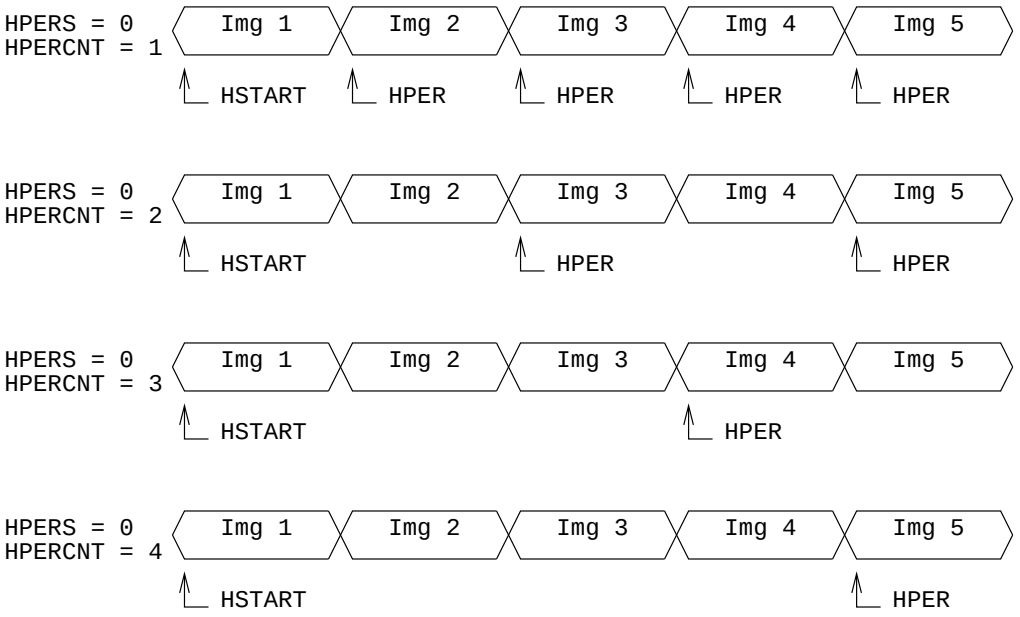


Figure 4-2: HPER[3:0] Insertion When HPERS = 0

The following example shows how often the HPER[3:0] header is inserted when HPERS = 1 with various HPERCNT[15:0] values. Like Fig. 4-2, HSTART again overrides HPER for the first segment. The setting of HO will override any header configuration, as in segment 4 (“Seg 4”) in the top graph. Note that the bottom two graphs show different image sizes.

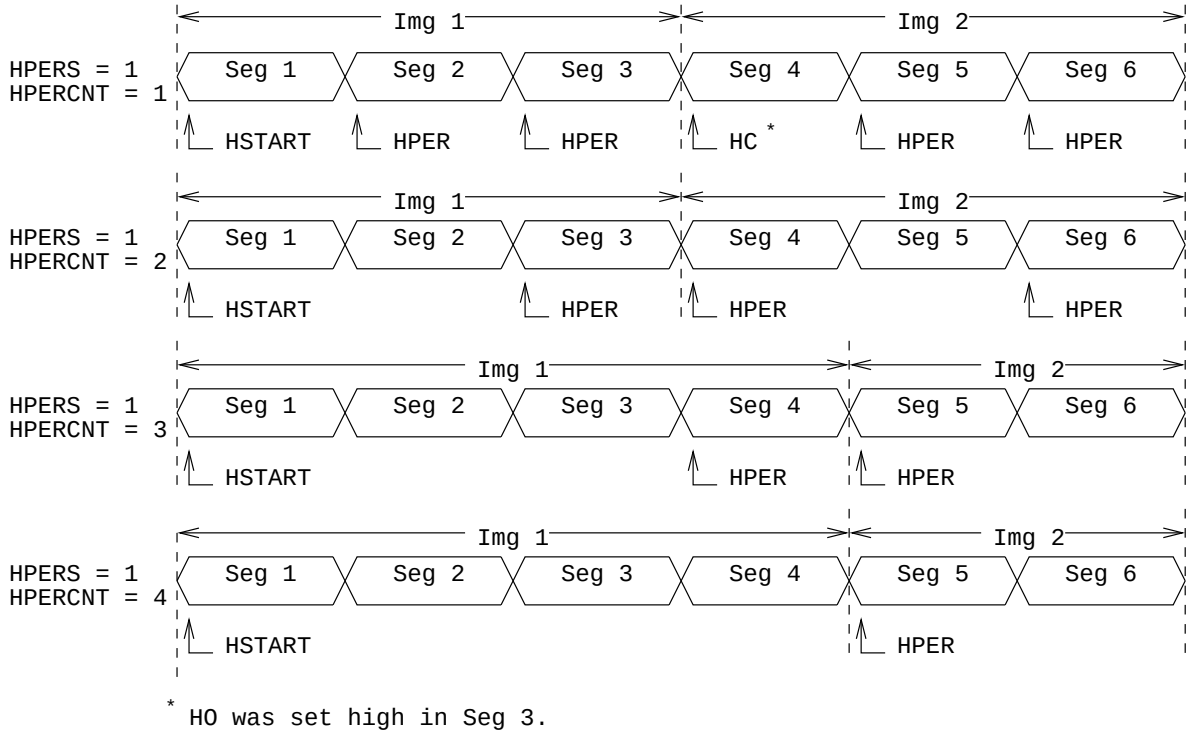


Figure 4-3: HPER[3:0] Insertion When HPERS = 1

HPERCNT[15:0]—Header Periodic Counter

Specifies the number of images or segments (depending on HPERS) between insertions of the HPER headers, modulo 2^{16} ($0 < HPERCNT <= 2^{16}$). Note that if the user changes HPERCNT during an image to a value which is less than the current segment or image count (depending on HPERS), HPER will be output on the next segment (if HPERS = 1) or the next image (if HPERS = 0), and the internal counter will reset. It will then count up to the new value of segments or images (depending on HPERS). If the user changes HPERCNT to a value which is higher than the current segment or image count, then the internal counter will continue counting, passing the old value, and incrementing up to the new HPERCNT value. HPER will be output when the counter equals the new HPERCNT value. Thereafter, the new HPERCNT value will be used to control HPER insertion.

HTYP[3:0]—Header Typical

If none of the previous header configurations are inserted, this becomes the default header configuration.

APPROX—Approximate Rate Output

When set high, coded bit-stream output is truncated at a certain stage quality (specified by the STGST parameter) *once* ROUT is reached. An exception is if ROUT is set to a value less than that required to output the DC minimum condition (DC quantized data plus any uncoded DC data per section 4.3.3 of reference [1]). In this case, the minimum data condition is output per section 3.6.2. If ROUT is reached in a particular bit-plane and within that bit-plane the stage quality set by the user has already been output, then the current coding stage is completed before the bit-stream is truncated. If a lossless condition is reached and FILL is set high, bit-stream output will continue until ROUT is met. Note that the APPROX parameter is not supported by reference [1].

ZIG—Zig-Zag Input order

If set high, indicates to the BPE that transform blocks (64 coefficients) are being input through the D[23:0] bus in zig-zag order. If low, the input order is interpreted in raster order. For specifics on input ordering see section 3.4.

NB[4:0]—Number of Bit-Planes Encoded

This parameter specifies the maximum quantization of the transform coefficient data in a segment or image, including the sign bit. NB[4:0] basically marks the location of the sign bit in the incoming 2s complement coefficient data. For example, if NB = 19, the sign bit for the incoming coefficient exists at pin D[18]. Therefore, any bit-plane data above NB - 1 is ignored. For users uncertain about the quantization of the transform data, refer to reference [2] to choose NB values for different transforms. At the minimum, the user must select an NB value consistent with NTYPE and R16.

NTYPE[1:0]—Type of NB

This parameter allows the BPE to make efficient use of the external RAM and thus increase the maximum pixels allowed per segment. This parameter also specifies the maximum number of bit-planes that will be encoded (parameter NB). When R16 = 1, NTYPE must be set to 2 (NB <=15). When R16 = 0, NTYPE may be any of the values below depending on NB:

NTYPE	***NB***
0	<= 24
1	<= 17
2	<= 15
3	<= 23

RAM[3:0]—External RAM Configuration

RAM[3:0]	*External RAM Word Depth*	*Maximum Pixels Per Segment NTYPE (R16)*				
		2(1)	*2(0)*	*1(0)*	*3(0)*	*0(0)*[1]
0	32k	16k	24k	20k	16k	16k
1	128k	64k	96k	80k	64k	64k
2	2k	1k	1.5k	1.25k	1k	1k
3	4k	2k	3k	2.5k	2k	2k
4	8k	4k	6k	5k	4k	4k
5	16k	8k	12k	10k	8k	8k
6	32k	16k	24k	20k	16k	16k
7	64k	32k	48k	40k	32k	32k
8	128k	64k	96k	80k	64k	64k
9	256k	128k	192k	160k	128k	128k
10	512k	256k	384k	320k	256k	256k
11	1M	512k	768k	640k	512k	512k
12	2M	1M	1.5M	1.25M	1M	1M
13	4M	2M	3M	2.5M	2M	2M
14	8M	4M	6M	5M	4M	4M
15	16M	8M	12M	10M	8M	8M

Table 4-3: Maximum pixels given parameters RAM, NTYPE, and R16

[1] This configuration is recommended when using the DWT decorrelator in reference [1].

The RAM[3:0] parameter indicates the word depth of the external RAM connected to the BPE and, in addition to parameters NTYPE[1:0] and R16, specifies the maximum pixels allowed per segment. Table 4-3 shows the relationship between these three parameters and how they affect maximum pixel count. Table 4-3 was developed using equations 4.3.1, 4.3.2, and 4.3.3. RAM word width has only two possible values, 16 or 24, as specified by the R16 parameter.

When NTYPE = 2 and R16 = 0:

Maximum Pixels = RAM Word Depth / 2 + 50% (4.3.1)

When NTYPE = 1 and R16 = 0:

Maximum Pixels = RAM Word Depth / 2 + 25% (4.3.2)

In all other cases:

Maximum Pixels = RAM Word Depth / 2 (4.3.3)

R16—RAM Width 16 Bits

When set high, specifies that the external RAM width is 16 bits; otherwise RAM width is 24 bits. When RAM width is set to 16 bits, only the 16 LSBs of the RIO[23:0] bus are used. Also, when R16 is set high, NTYPE[1:0] must equal 2 and NB[4:0] must be less than or equal to 15.

RAMA—RAM A Only

When set high, this forces the BPE to use external RAM A only. The BPE will use the RNCSA, RNWEA, RNOEA, RADDA[23:0], and RIOA[23:0] pins to access RAM A. Since the BPE will use only one RAM, there must be gaps or wait states between input segments to allow the BPE to read data from RAM A once it's been written. For specifics on this mode see section 3.5.

JA[1:0]—BPE J Blocks

When the BPE is analyzing the input data for the best coding option, it does so across a user-specified number of transform blocks. Parameter JA[1:0] specifies the number of blocks. JA must be set to 0 (16 transform blocks) in order to conform to reference [1].

JA	***Blocks***
0	16
1	24
2	8
3	32

JU[1:0]—DC ENCODER J Samples

This indicates the number of DC samples per gaggle required for the DC ENCODER (see Fig. 1-1), which is internal to the BPE. JU must be set to 0 (16 samples per block) in order to conform to reference [1], section 4.3.2.5.

JU	***Samples***
0	16
1	10
2	8
3	16

UMAP—User Mappings

When set high, implies that the user has specified mappings via the MAP4[63:0], MAP3[23:0], or MAP2[7:0] parameters that differ from reference [1]. When low, the BPE uses mappings per reference [1].

MAP4[63:0]—4-Bit Mappings

When UMAP is set high, MAP4 specifies the 4-bit symbol mappings. Mapping bits for parameter MAP4—as well as MAP3 and MAP2—are ordered such that the higher order symbols are positioned toward the MSBs. For example, the bits at
MAP4[63:60] represent the 4-bit symbol to which the “all ones” conditions will be mapped. MAP4[3:0] contains the bits to which the “all zeros” condition will be mapped.

MAP3[23:0]—3-Bit Mappings

When UMAP is set high, MAP3 specifies the 3-bit symbol mappings.

MAP2[7:0]—2-Bit Mappings

When UMAP is set high, MAP2 specifies the 2-bit symbol mappings.

TEST[3:0]—Test Mode

When used in conjunction with the TE pin, this parameter determines the BPE test mode. During normal operation, this parameter must be zeroed.

4.4 Applying Weights

The BPE has the capability to apply frequency specific weights per reference [1]. Weighting incoming coefficients invokes a left-shift, thereby multiplying the appropriate data by one, two, four, or eight, and possibly removing MSBs. Table 4-4 shows the interaction of the parameters UWTS and DWT. UWTS, DWT, and the weights are set using the PINT or SINT.

UWTS	***DWT***	***Weights Used***	***Notes***
0	0	N/A	Recommended configuration when using floating point DWT[1]
0	1	Default	Recommended configuration when using integer DWT
1	0	User	Not supported by reference [1][2]
1	1	User	Apply user-defined weights when using integer DWT

Table 4-4: Parameters That Control Weight Application

[1] This mode is only valid when NB is less than or equal to 21.
[2] When using floating point DWT, and when NB is greater than 21, this mode may be used to set WDC to satisfy Eqn 3.4.1.

4.5 Dynamic Updating of Parameters

Due to the flexibility of the serial and parallel interfaces, it is possible to update BPE initialization parameters dynamically, provided the user adheres to some restrictions. Most parameters can be updated, but not all updates take effect during the following segment. For example, the “once at the beginning of an image” parameters (hereafter called “image parameters”) can be updated during any segment. However, the changes which may have occurred in the image parameters, though effected via the PINT or SINT in the current segment, will not take effect until the start of the next image. Further, certain parameters are never meant to change such as RAM[3:0], NTYPE[1:0], RAMA, and R16. These parameters are precluded from updating once BPE processing begins.

The following parameters can change every segment:

EI, NB[4:0], S[19:0],
APPROX, DCST, BPST[4:0], STGST[1:0], FILL, ROUT[23:0],
HO, HC[3:0], HSTART[3:0], HTYP[3:0], HPER[3:0], HPERS, HPERCNT[15:0],
RES1[5:0], RES2[3:0], RES3[1:0]

The following parameters can only change once at the beginning of an image:

IGSEG, ISEG[15:0], RES4[13:0],
DWT, PADROW[2:0], SIGN, N[3:0], WID[19:0], TPOSE,
RES4[13:0],
UWTS,
WDC[1:0], WP0[1:0], WP1[1:0], WP2[1:0], WC0[1:0], WC1[1:0],
WC2[1:0], WG0[1:0], WG1[1:0], WG2[1:0]

The following parameters must *never* change once BPE processing begins:

RAM[3:0], NTYPE[1:0], JA[1:0], JU[1:0], R16, RAMA, ZIG, UMAP, MAP4[63:0], MAP3[23:0],
MAP2[7:0], TEST[3:0]

It is recommended that the host controller use the provided segment markers, SOS and EOS, to avoid data transfer conflicts when dynamically updating parameters (see timing in sections 6.8 and 6.9). When using the PINT, all read/write activity can occur at anytime. However, the controller must signal an update (by asserting the PUPD pin) at least T_{UHSS} cycles before the start of the segment to which those parameters will be applied. Further, PUPD assertion must be precluded for T_{SSUH} cycles after the start of any given segment. When operating the SINT, the serial bit-stream cannot be stalled across segment boundaries, and therefore, the 304th valid serial bit must be passed T_{ELSS} cycles before the start of a segment. Moreover, SINT usage cannot begin until T_{SSEH} cycles after the start of a segment. If the the input data stream is continuous, the SOS and EOS pins are asserted during this "parameter preclusion period" and the host controller can use these two pins to know when *not* to signal an update. However, due to the possibility of wait states or stalled input data (DVALID = 0) occurring between segments, the preclusion period may not be accurately represented by SOS and EOS. (EOS could drop low followed by an unknown amount of wait states before SOS is asserted.) In this case, the host controller must either keep track of the preclusion period or simply update during guaranteed safe periods, such as immediately after SOS drops low.

5.0 Package, Pin Assignments and Function Descriptions

5.1 Aeroflex 256-pin CQFP (44182)

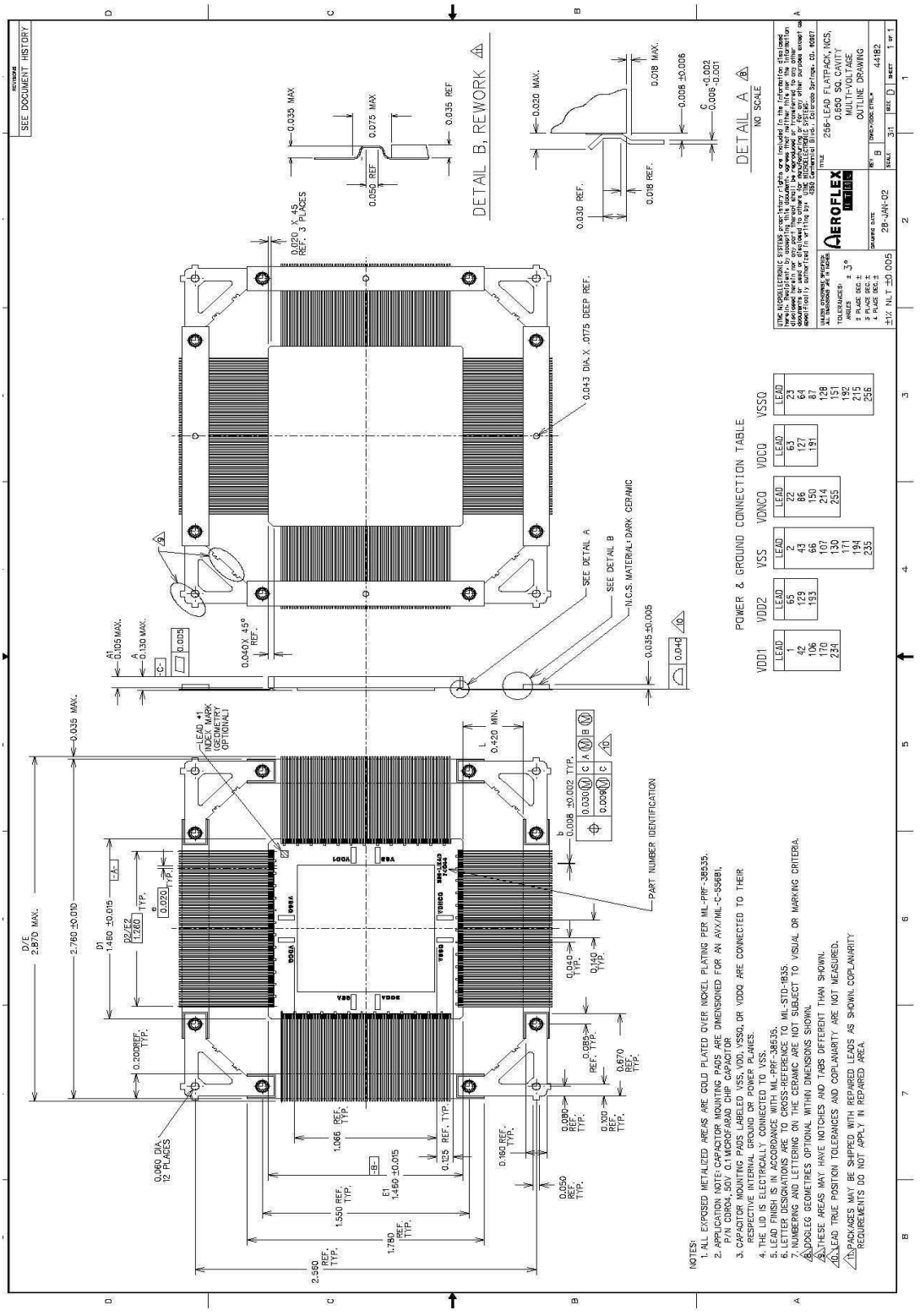


Figure 5-1: Flight-qualified Package

5.2 Pin Assignments[1]

Pin	*Pad*	*Signal*	*Pin*	*Pad*	*Signal*	*Pin*	*Pad*	*Signal*	*Pin*	*Pad*	*Signal*
1		VDD	33		RADDB_2	65		VDD	97		RADDA_6
2		VSS	34		RIOA_23	66		VSS	98		NC
3		RADDB_20	35		RADDB_0	67		RIOA_2	99		NC
4		NC	36		RIOA_22	68		RIOA_1	100		DVDD
5		RADDB_19	37		NC	69		RNCSA	101		RADDA_5
6		NC	38		RIOA_21	70		RIOA_0	102		RADDA_4
7		NC	39		RIOA_20	71		RNOEA	103		RADDA_3
8		RADDB_18	40		RIOA_19	72		RNWEA	104		VDD
9		RADDB_16	41		VDD	73		DVDD	105		VDD
10		RADDB_17	42		VDD	74		RADDA_22	106		VDD
11		NC	43		VSS	75		RADDA_23	107		VSS
12		RADDB_15	44		RIOA_18	76		RADDA_21	108		RADDA_1
13		NC	45		RIOA_16	77		RADDA_20	109		RADDA_2
14		RADDB_14	46		RIOA_17	78		RADDA_19	110		DVDD
15		RADDB_13	47		RIOA_15	79		RADDA_18	111		RADDA_0
16		RADDB_12	48		DVDD	80		DVDD	112		VDD
17		RADDB_10	49		RIOA_14	81		RADDA_16	113		D_1
18		NC	50		RIOA_12	82		RADDA_17	114		D_0
19		RADDB_11	51		RIOA_13	83		RADDA_15	115		D_2
20		RADDB_9	52		RIOA_10	84		NC	116		D_3
21		DVDD	53		RIOA_11	85		RADDA_14	117		D_4
22		DVDD	54		DVDD	86		DVDD	118		D_5
23		DVSS	55		RIOA_9	87		DVSS	119		D_6
24		NC	56		RIOA_7	88		RADDA_12	120		D_8
25		RADDB_8	57		RIOA_8	89		RADDA_13	121		D_7
26		RADDB_7	58		RIOA_6	90		VDD	122		D_9
27		RADDB_6	59		VDD	91		RADDA_11	123		D_10
28		RADDB_4	60		RIOA_5	92		RADDA_9	124		D_11
29		RADDB_5	61		RIOA_3	93		RADDA_10	125		D_12
30		RADDB_3	62		RIOA_4	94		RADDA_7	126		D_13
31		DVDD	63		DVDD	95		RADDA_8	127		DVDD
32		RADDB_1	64		DVSS	96		VDD	128		DVSS

Table 5-1: Pin Assignments

Pin	Pad	Signal	Pin	Pad	Signal	Pin	Pad	Signal	Pin	Pad	Signal
129		VDD	161		VDD	193		VDD	225		NC
130		VSS	162		PIO_3	194		VSS	226		RIOB_15
131		D_15	163		PIO_4	195		Q_10	227		RIOB_14
132		D_14	164		PIO_6	196		Q_11	228		RIOB_13
133		D_16	165		PIO_5	197		Q_8	229		RIOB_12
134		NC	166		PIO_7	198		Q_9	230		NC
135		D_17	167		ALE_CLK	199		Q_6	231		VDD
136		D_18	168		DVDD	200		Q_7	232		NC
137		D_19	169		PACK	201		Q_5	233		RIOB_11
138		D_20	170		VDD	202		DVDD	234		VDD
139		D_21	171		VSS	203		Q_3	235		VSS
140		D_22	172		SCC	204		Q_4	236		RIOB_10
141		D_23	173		PUPD	205		Q_1	237		RIOB_9
142		DVALID	174		SCE	206		Q_2	238		RIOB_8
143		SOS	175		TE	207		Q_0	239		RIOB_7
144		DEOI	176		SCD	208		DVDD	240		RIOB_6
145		EOS	177		VDD	209		RIOB_23	241		DVDD
146		NC	178		RESETN	210		RIOB_22	242		RIOB_5
147		EOIS	179		REQ	211		RIOB_21	243		RIOB_4
148		DVDD	180		QFILL	212		NC	244		RIOB_3
149		PMODE	181		QEOS	213		NC	245		RIOB_2
150		DVDD	182		QRTRIG	214		DVDD	246		RIOB_1
151		DVSS	183		QSOS	215		DVSS	247		RIOB_0
152		PUMODE	184		DVDD	216		VDD	248		DVDD
153		PIEN	185		QRDY	217		RIOB_19	249		RNWEB
154		PWRN	186		Q_14	218		RIOB_20	250		RNOEB
155		PIO_0	187		Q_15	219		RIOB_18	251		RADDB_23
156		PRDN	188		Q_12	220		RIOB_17	252		RNCSB
157		PIO_2	189		Q_13	221		NC	253		RADDB_21
158		DVDD	190		DVDD	222		RIOB_16	254		RADDB_22
159		PIO_1	191		DVDD	223		NC	255		DVDD
160		CLK	192		DVSS	224		VDD	256		DVSS

Table 5-1: Pin Assignments

[1] NC means “no-connect.” Pins that are NC must be left floating.

5.3 Pin Function Descriptions

Pin[1, 2]	***Pins Used***	***I/O***	***Description***
RESETN	1	I	Reset, active low. When active, this pin causes BPE reset. RESETN should be active for T_{RST} cycles per section 6.4. Upon exiting reset, all input control signals must be in valid states.
CLK	1	I	BPE Input Clock. Data synchronous to CLK is clocked on the rising edge. CLK must be cycling during reset.
SCC	1	I	Serial Interface Input Clock. SCC can be asynchronous to CLK, but must be synchronized with data at the SCE and SCD pins. Data synchronous to SCC is clocked on the rising edge. SCC must be cycling during reset.
ALE_CLK	1	I	8051 Address Latch Enable (ALE) or FPGA Input Clock. This signal is asynchronous to CLK and is used to clock initialization data into the parallel interface (PINT). In PINT mode 0 (PMODE = 0), this pin receives the ALE signal from the 8051 (or equivalent). In PINT mode 1 (PMODE = 1), this pin receives the input clock signal from a device which supports synchronous, byte-per-clock data transfers. (FPGA or equivalent). ALE_CLK does *not* have to cycle during reset.
PMODE[3]	1	I	Parallel Interface Mode. This pin indicates which host controller is interacting with the BPE. PMODE = 0 implies 8051, PMODE = 1 implies any device which supports synchronous, byte-per-clock data transfers (FPGA or equivalent).
PUMODE	1	I	Parallel Interface Update Mode. This port indicates how the host controller should interpret the PACK signal. If PUMODE = 1, the PINT will assert high the PACK pin once the PINT block senses an active high PUPD signal internally. If PUMODE = 0, the PINT will assert the PACK pin once the PUPD signal has been received *and* all parameters from the PINT have been passed to the BPE internals.
PIEN	1	I	Parallel Interface Enable, active low. When active, this pin enables the host controller to write to and read from the PINT, unless the BPE is currently reading parameters from the PINT. In the latter case, the PIEN pin—and thus all host controller reading and writing—is inhibited. It is not necessary to activate the PIEN pin when signaling a parameter update with the PUPD pin.
PWRN	1	I	Parallel Interface Write Enable, active low. This pin signals a PINT write.
PRDN	1	I	Parallel Interface Read Enable, active low. This pin signals a PINT read.
PIO[7:0]	8	IO	Parallel Interface Input/Output Bus. This bi-directional bus is used to pass BPE parameters to and from the PINT. During an active PIEN and PRDN, the BPE output drivers will drive this bus; in all other cases, the host controller must drive this bus. See the following chart: PIEN PWRN PRDN PIO Bus Status 1 X X High-Z 0 0 X High-Z 0 1 0 Output 0 1 1 High-Z

Pin[1, 2]	***Pins Used***	***I/O***	***Description***
PUPD	1	I	Parallel Interface Update. An active PUPD indicates that BPE parameters which currently reside in the PINT should now be passed to the BPE internals. The PUPD signal must be be held active until the PACK is asserted. An active PUPD must not occur during the SOS and EOS segment markers. It is not necessary to assert the PUPD pin when using the serial interface.
PACK	1	O	Parallel Interface Update Acknowledge. Asserted high, synchronous to CLK, when: 1). PUMODE = 1 and an active PUPD is sensed internally by the BPE, or 2). PUMODE = 0 and an active PUPD is sensed *and* the current PINT parameters have been passed to the BPE internals.
SCE[4]	1	I	Serial Interface Enable. When active, synchronous to SCC, signals that the data bit on the SCD pin is valid.
SCD	1	I	Serial Interface Input Data. This pin is used to transfer 1-bit data to the serial interface (SINT), synchronous to SCC. To enable the SINT, the first bit of data in a complete 304 SCC cycle transfer must always be a one.
DVALID	1	I	Data Input Valid. When active, synchronous to CLK, this pin indicates that coefficient data on the D[23:0] bus is valid. Data input is stallable, so DVALID does not have to be high for a minimum number of CLK cycles.
D[23:0]	24	I	Data Input Bus. This is the bus used to pass right-justified coefficient data to the BPE, synchronous to CLK.
DEOI	1	I	Data Input End of Image. When active, synchronous to CLK, this pin signals that the current segment is the last in an image. It may be a pulse or otherwise, but must occur between or during SOS and EOS. That is, this pin is ignored after the end of a segment, but will be re-sampled once another segment has begun. An active DEOI pin overrides any image or segment counting which occurs when using the BPE parameters IGSEG and ISEG. DVALID does not have to be active for the BPE to sense DEOI.
SOS	1	O	Start of Segment. This output pin is asserted high one CLK cycle after the beginning of an input segment and is held high for 64 valid data transfers. Its main purpose is to provide timing information for updating BPE parameters.
EOS	1	O	End of Segment. This output pin is asserted high one CLK cycle after the beginning of the last transform block in an input segment and is held high for 64 valid data transfers. Its main purpose is to provided timing information for updating BPE parameters.
EOIS	1	O	End of Image Segment. Generally, this is asserted high during the last segment in an image. However, the timing for this pin varies depending on DEOI activity and the BPE parameters EI, IGSEG and ISEG. This pin provides the user with an image marker.
RNCSA(B)[5]	1	O	RAM A(B) Chip Select, active low.
RNWEA(B)	1	O	RAM A(B) Write Enable, active low.
RNOEA(B)	1	O	RAM A(B) Output Enable, active low.

Pin[1, 2]	***Pins Used***	***I/O***	***Description***
RADDA(B) [23:0]	24	O	RAM A(B) Address Bus.
RIOA(B)[23:0]	24	IO	RAM A(B) Data Bus. The BPE always drives this bus unless a RAM read is requested by the BPE.
QRDY	1	O	Data Output Ready. When asserted high indicates that data on the Q output bus is ready. The QRDY signal will remain high as long as there is data in the BPE's output FIFO. The REQ pin must be active and QRDY must be high for valid data transfer.
Q[15:0]	16	O	Data Output Bus. The output bus used to transfer left-justified data to the downstream device. The LSBs of the bus, if not used, are filled with zeros. Data output is stallable using the REQ pin.
QFILL	1	O	Data Output Fill. When asserted high indicates that the current output word consists of nothing but fill bits (zeros). The BPE FILL parameter must be set in order for this pin to function. Both the QRDY and REQ pins must be high in order for QFILL to be asserted.
QRTRIG	1	O	Data Output Rate Trigger. This pin is pulsed high one CLK cycle when the current output word meets the rate output specified by BPE ROUT parameter. Both the QRDY and REQ pins must be high in order for QRTRIG to be asserted.
QSOS	1	O	Data Output Start of Segment. This pin is pulsed high one CLK cycle coincident with the first output word in a segment. Both the QRDY and REQ pins must be high in order for QSOS to be asserted.
QEOS	1	O	Data Output End of Segment. This pin is pulse high one CLK cycle coincident with the last output word in a segment. Both the QRDY and REQ pins must be high in order for QEOS to be asserted.
REQ	1	I	Data Output Request. When active, synchronous to CLK, signals to the BPE that the downstream device desires data. Although REQ may be active, data may not be immediately available (QRDY = 0). This would only occur if the BPE's output FIFO was empty. Otherwise, if there exists data in the output FIFO, this data will be made immediately available (QRDY = 1).
TE	1	I	Test Enable. This pin is used for packaged parts testing in conjunction with the BPE TEST parameter. This pin must be tied low during normal operation of the BPE.

Table 5-2: Pin Function Descriptions

[1] Unless specified, input control pins are active high.
[2] Unused input pins should be tied high or low, whichever is appropriate. Unused bi-directional pins should have weak pull-ups (or pull-downs).
[3] For details on the parallel interface, see section 3.2.
[4] For details on the serial interface, see section 3.3.
[5] For details on the RAM interface, see section 3.5.

6.0 Specifications

6.1 Absolute Maximum Ratings

Parameter	*Description*	*Range*	*Unit*
V_{DD}	Max. voltage between core voltages V_{DD} and V_{SS}	-0.3 to +2.95	V
V_{DVDD}	Max. voltage between IO voltages V_{DVDD} and V_{DVSS}	-0.3 to +3.8	V
$V_{I/O}$	Max. voltage on any given pin	-0.3 to +3.8	V
F_{MAX}	Max. frequency	20	MHz
T_{STG}	Storage temperature	-65 to +150	ºC
T_J	Max. junction temperature	150	ºC

Table 6-1: Absolute Maximum Ratings

6.2 Recommended Operating Conditions

Parameter	*Description*	*Range*	*Unit*
V_{DD}	Operating voltage, core	2.25 to 2.75	V
V_{DVDD}	Operating voltage, IO	3.0 to 3.6	V
T_J[1]	Operating junction temperature range	-55 to +110	ºC
R_{JA}	Thermal junction to ambient resistance	6.0	ºC/W
R_{JC}	Thermal junction to case resistance	4.5	ºC/W

Table 6-2: Recommended Operating Conditions

[1] Note that T_J can be raised by lowering F_{MAX}. Lowering F_{MAX} to 13MHz allows T_J to rise to 125ºC; lowering F_{MAX} still further, to 7MHz, allows T_J to rise to 150ºC.

6.3 Electrical Characteristics[1]

Parameter	*Description*	*Min*	*Typ*	*Max*	*Unit*	*Notes*
V_{IH}	Min. high level input voltage	0.7 x V_{DVDD}			V	
V_{IL}	Max. Low level input voltage			0.3 x V_{DVDD}	V	
V_{IHC}	Min. high level input voltage, high clock input	0.7 x V_{DVDD}			V	
V_{ILC}	Max. low level input voltage, low clock input			0.3 x V_{DVDD}	V	
V_{OH}	High level output voltage	2.35			V	I_{OH} = -30.0mA
V_{OL}	Low level output voltage			0.6	V	I_{OL} = 30.0mA
I_{IH}	High level input leakage	-1		1	uA	V_{IN} = V_{DVDD}
I_{IL}	Low level input leakage	-1		1	uA	V_{IN} = V_{DVSS}
I_{VDD}[2]	Operating current, core		0.23	0.42	A	
I_{DVDD}[2]	Operating current, IO		0.02	0.2	A	
QI_{DD}	Quiescent current, core		120	600[3]	uA	
QI_{DVDD}	Quiescent current, IO		10	300[3]	uA	

Table 6-3: Electrical Characteristics

[1] Operating conditions: V_{DVDD} = 3.3V ± 10%, V_{DVSS} = 0V, V_{DD} = 2.5V ± 10%, V_{SS} = 0V, T_J = -55ºC to +110ºC

[2] Both core and I/O dynamic current greatly depend on the quantization and correlation of the coefficient input data. The typical current numbers came from compressing the sar16bit image of reference [2]. The maximum current numbers were produced using 24-bit random coefficient data (incompressible). Both current numbers assume F = 20MHz.

[3] Current numbers assume an absorbed total dose of 50krad (Si) at 25°C, applied at dose rates below 20millirads/s. Also note that, due to internal RAM pre-charge functionality, the CLK signal must be stopped high to properly test QI_{DD}.

6.3.1 Power Cycling

On BPE power-up, to avoid high current states, V_{DD} power must be applied either before or during the initial application of V_{DVDD}. Soon after, if not coincident with V_{DVDD} application, assert at least one rising edge clock edge on CLK.

6.4 Clock Specifications

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{CLKW}	Core Clock (CLK) Period	50		ns
T_{SCCW}	Serial Interface Clock (SCC) Period	50		ns
T_{ALEW}[1]	Parallel Interface Clock (ALE_CLK) Period	50		ns
T_{CLK0}	CLK Zero Time	20		ns
T_{CLK1}	CLK One Time	20		ns
T_{SCC0}	SCC Zero Time	20		ns
T_{SCC1}	SCC One Time	20		ns
T_{ALE0}[1]	ALE_CLK Zero Time	20		ns
T_{ALE1}[1]	ALE_CLK One Time	20		ns
T_{CKRF}	CLK, SCC, ALE_CLK Rise and Fall Times		2	ns

Table 6-4: Clock Specifications

[1] T_{ALEW}, T_{ALE0}, and T_{ALE1} apply only when PMODE = 1.

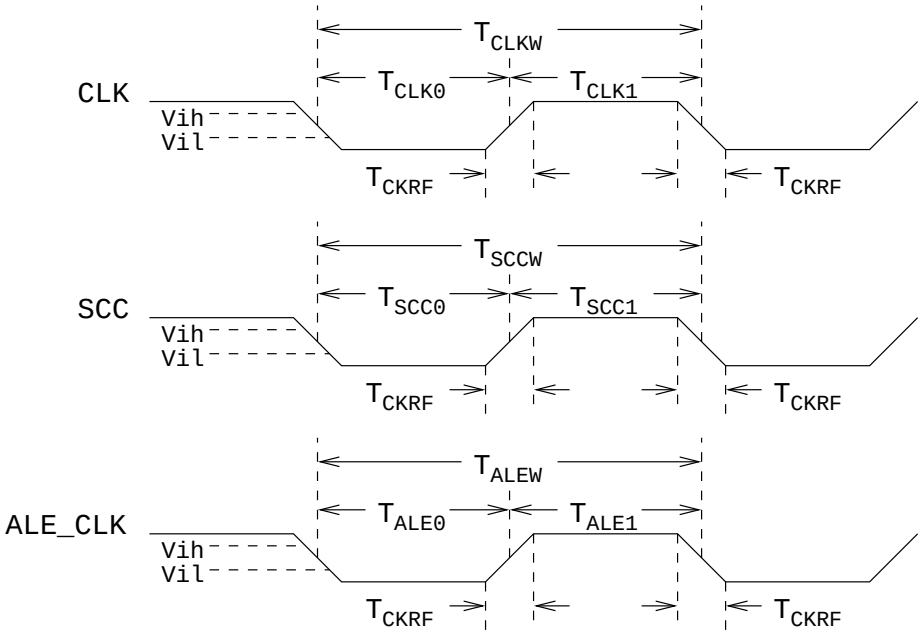


Figure 6-1: Input Clocks

6.5 RESETN and BPE Initialization Specifications

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{RST}	RESETN Width Low	10		cycles[1]
T_{RSSU}	RESETN Setup to CLK High	22		ns
T_{RSHD}	RESETN Hold after CLK High	0		ns
T_{RSEH}	RESETN High to SCE High	1		CLK cycles
T_{ELSS}	SCE Low (304th Serial Bit) to Start of Segment	64		CLK cycles
T_{RSIE}	RESETN High to PIEN Low	1		CLK cycles
T_{UHSS}	PUPD High to Start of Segment	64		CLK cycles

Table 6-5: RESETN and BPE Initialization Specifications

[1] The slower of either CLK or SCC.

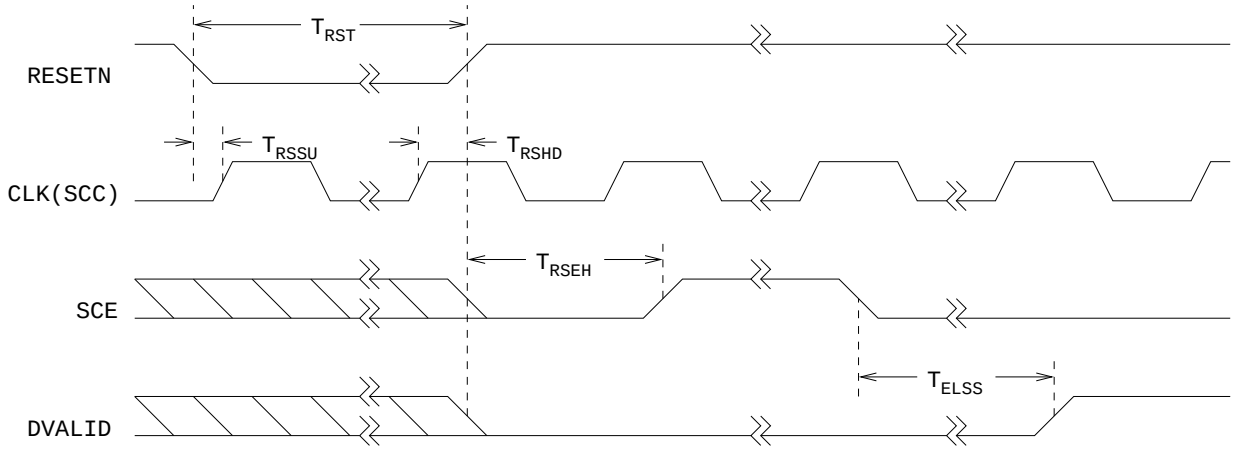


Figure 6-2: RESETN and BPE Initialization using the SINT

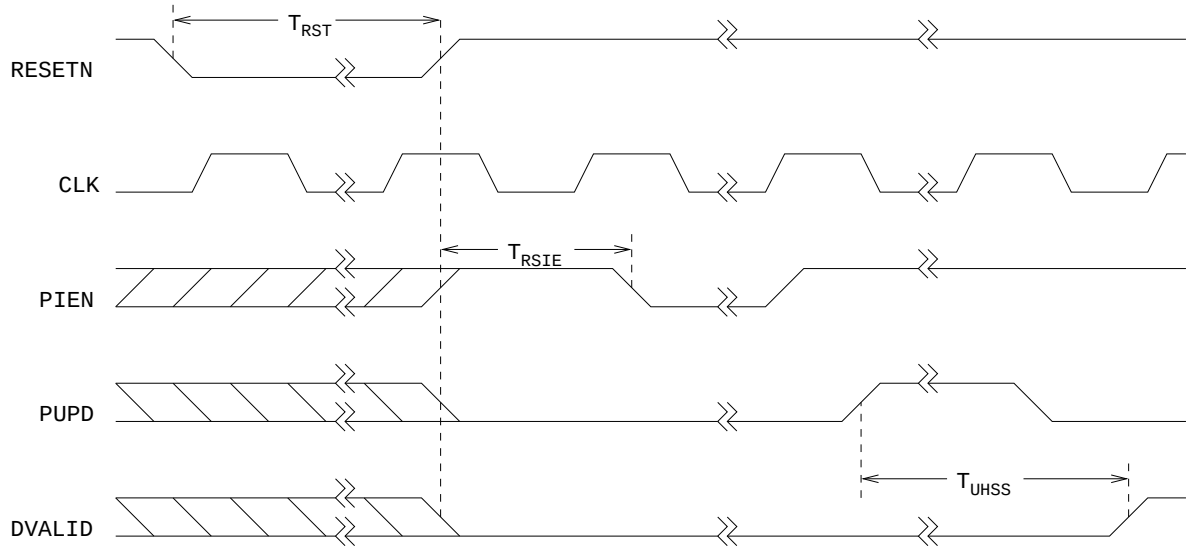


Figure 6-3: RESETN and BPE Initialization Using the PINT

6.6 Parallel Interface (PINT) Specifications

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{LHLL}	ALE_CLK One Time	10		ns
T_{ILAV}	PIEN Low to Address Valid	7		ns
T_{AVLL}	Address Setup to ALE_CLK Low	3		ns
T_{LLAX}	Address Hold after ALE_CLK Low	1		ns
T_{LLWL}	ALE_CLK Low to PWRN Low	1		ns
T_{DVWH}	Data Setup to PWRN High	4		ns
T_{WLWH}	PWRN Pulse Width	10		ns
T_{WHLH}	PWRN High to ALE_CLK High	0		ns
T_{WHDX}	Data Hold after PWRN High	2		ns
T_{WHIH}	PWRN High to PIEN High	2		ns

Table 6-6: PINT Mode 0 (PMODE = 0) Write Timing

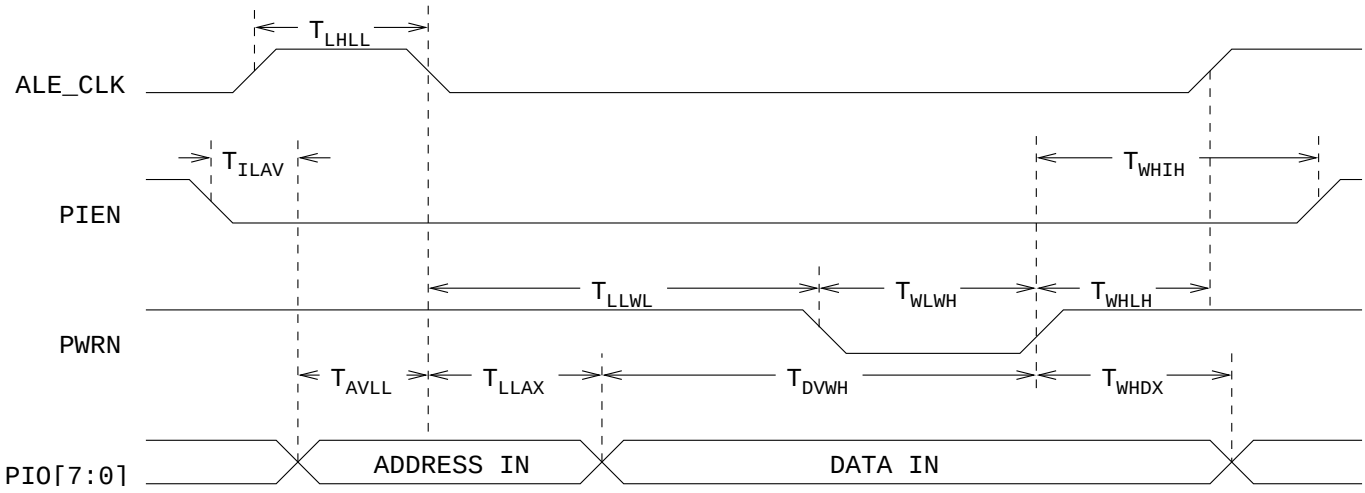


Figure 6-4: PINT Mode 0 Write Timing

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{LHLL}	ALE_CLK One Time	10		ns
T_{ILAV}	PIEN Low to Address Valid	7		ns
T_{AVLL}	Address Setup to ALE_CLK Low	3		ns
T_{LLAX}	Address Hold after ALE_CLK Low	1		ns
T_{AZRL}	Address Float to PRDN Low	0		ns
T_{RLQX}	PRDN Low to Data Transition	2	5	ns
T_{RLQV}	PRDN Low to Data Valid	2	7	ns
T_{RLRH}	PRDN Pulse Width	10		ns
T_{RHLH}	PRDN High to ALE_CLK High	0		ns
T_{RHQZ}	PRDN High to Data Float	2	6	ns
T_{RHIH}	PRDN High to PIEN High	2		ns

Table 6-7: PINT Mode 0 (PMODE = 0) Read Timing

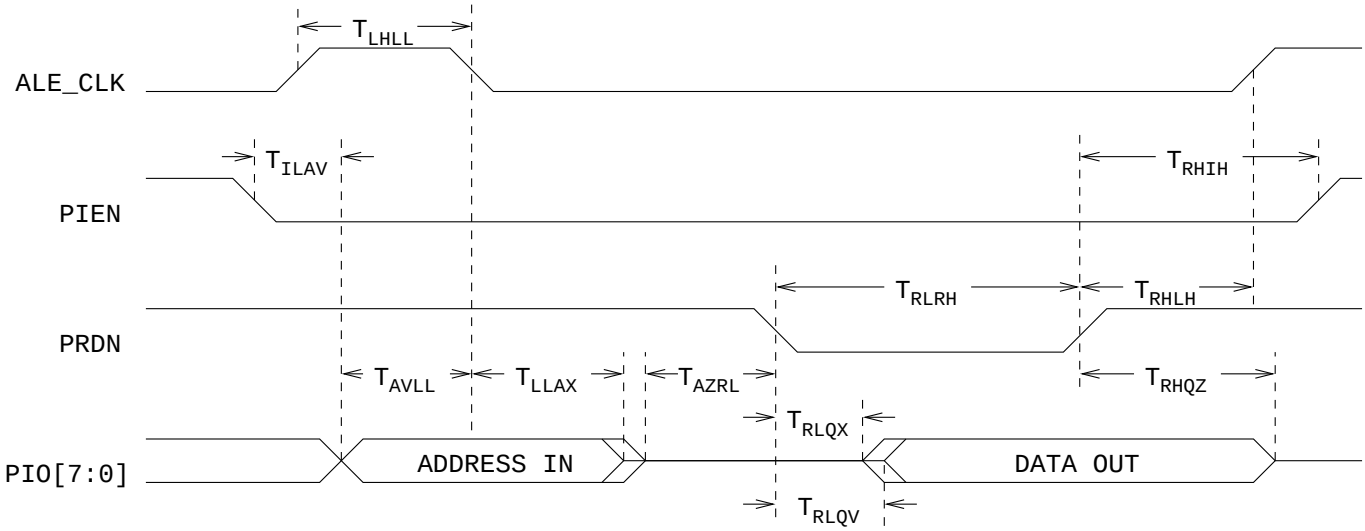


Figure 6-5: PINT Mode 0 Read Timing

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{IESU}	PIEN Setup to ALE_CLK High	5		ns
T_{WLSU}	PWRN Setup to ALE_CLK High	5		ns
T_{PDSU}	PIO Data Setup	5		ns
T_{WLHD}	PWRN Hold after ALE_CLK High	2		ns
T_{PDHD}	PIO Data Hold	2		ns
T_{IEHD}	PIEN Hold after ALE_CLK_High	2		ns

Table 6-8: PINT Mode 1 (PMODE = 1) Write Timing

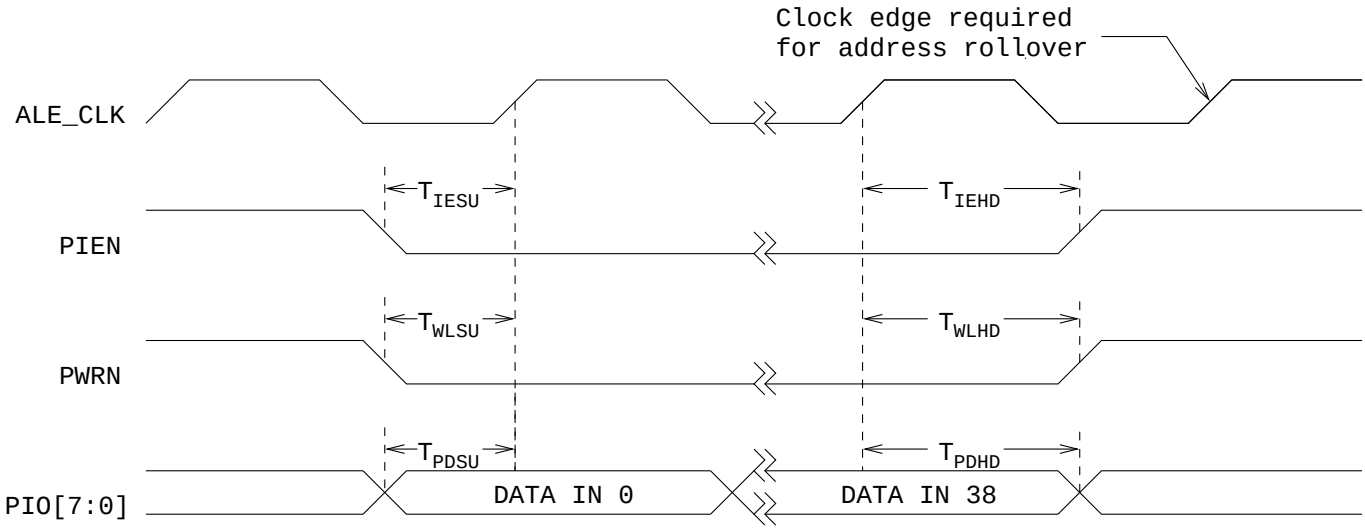


Figure 6-6: PINT Mode 1 Write Timing

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{RLSU}	PRDN Setup to ALE_CLK High	5		ns
T_{RLQX}	PRDN Low to Output Data Transition	2	5	ns
T_{RLQV}[1]	PRDN Low to Output Data Valid	2	7	ns
T_{RLHD}	PRDN Hold after ALE_CLK High	2		ns
T_{RHQZ}	PRDN High to Output Data Float	2	6	ns

Table 6-9: PINT Mode 1 (PMODE = 1) Read Timing

[1] Since there is no flip-flop boundary between the PINT RAM and the PIO bus, there is only a small delay between the time when PRDN first drops low (reading PINT address 0) and when valid data appears on the PIO bus. Therefore, to prevent destroying address 0 data, the user must not only satisfy T_{RLSU} but also allow T_{RLQV} for the development of address 0 data on the PIO bus.

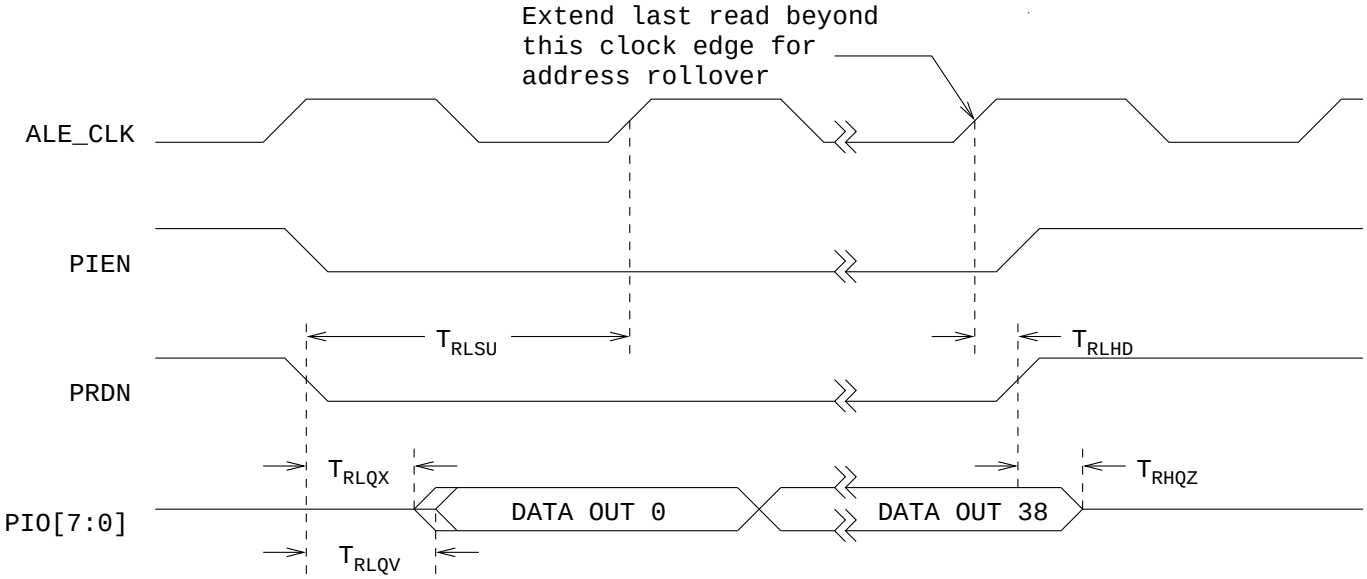


Figure 6-7: PINT Mode 1 Read Timing

6.7 Serial Interface (SINT) Specifications

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{SESU}	SCE Setup to SCC High	10		ns
T_{SDSU}	SCD Setup to SCC High	10		ns
T_{SEHD}	SCE Hold after SCC High	0		ns
T_{SDHD}	SCD Hold after SCC High	0		ns

Table 6-10: Serial Interface Timing

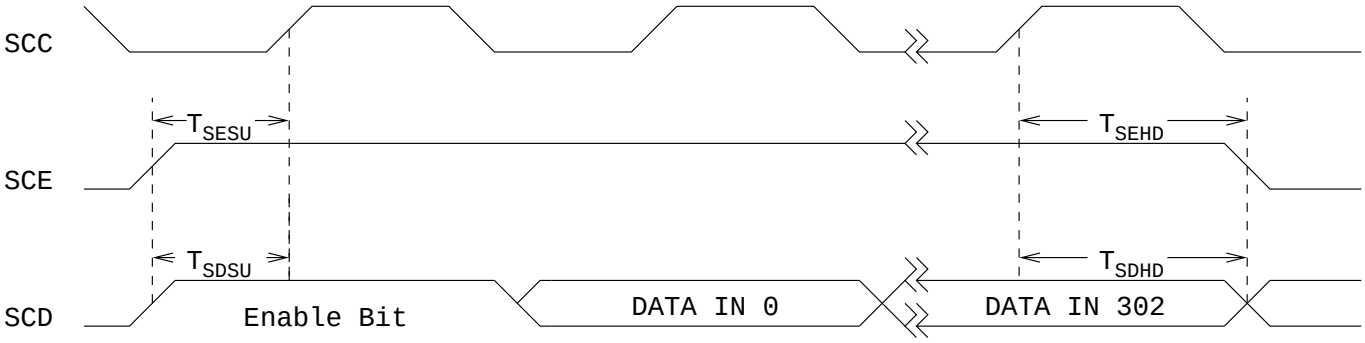
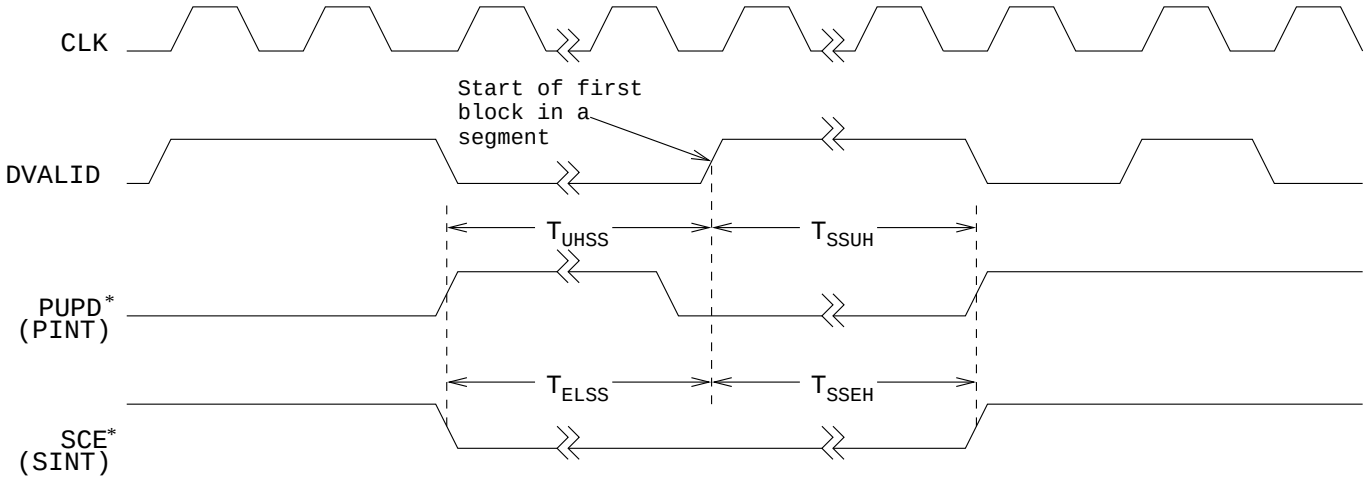


Figure 6-8: Serial Interface Timing

6.8 Dynamic Updating Specifications

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{UHSS}	PUPD High to Start of Segment	64		CLK cycles
T_{ELSS}	SCE Low (304th Serial Bit) to Start of Segment	64		CLK cycles
T_{SSUH}	Start of Segment to PUPD High	64		CLK cycles
T_{SSEH}	Start of Segment to SCE High (1st Serial Bit)	64		CLK cycles

Table 6-11: Dynamic Updating Restrictions



* Both interfaces are shown for illustrative purposes only. It is not recommended to operate both interfaces at once.

Figure 6-9: Dynamic Updating Preclusion Period

6.9 SOS (EOS) Assertion Specifications

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{ISGA}	SOS (EOS) Assertion/de-assertion Time	T_{CLKW} + 5	T_{CLKW} + 11	ns
T_{ISGW}	SOS (EOS) Pulse Width	note1	note 2	CLK cycles

Table 6-12: SOS and EOS Assertion Specifications

[1] T_{ISGW} minimum time is 64 CLK cycles.
[2] T_{ISGW} maximum time is 64 CLK cycles plus the number of stalled input data states (DVALID = 0) occurring in the first (last) block of a segment.

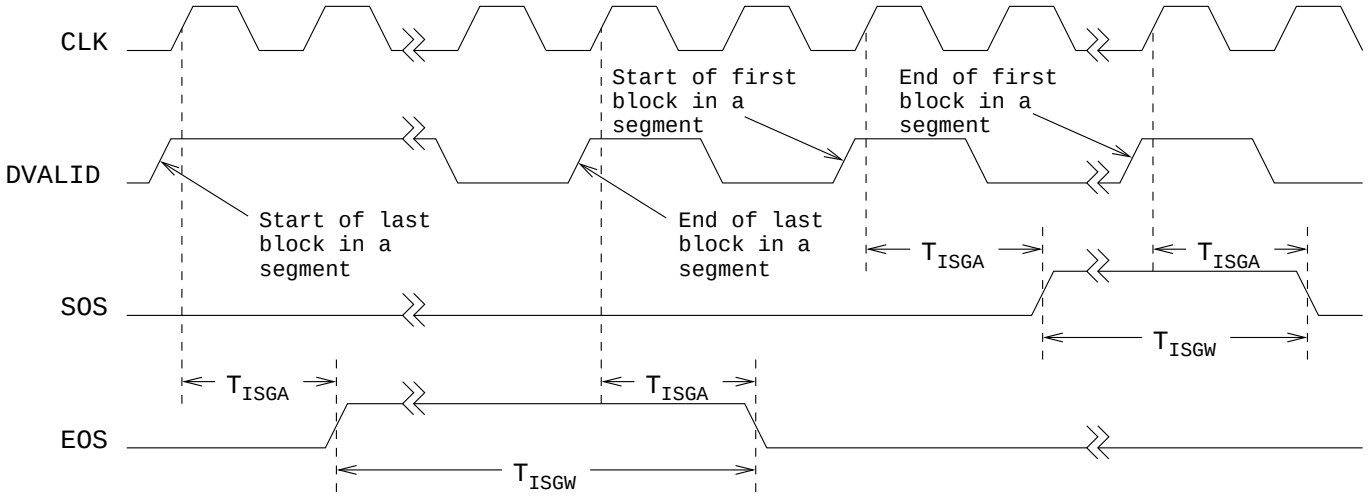


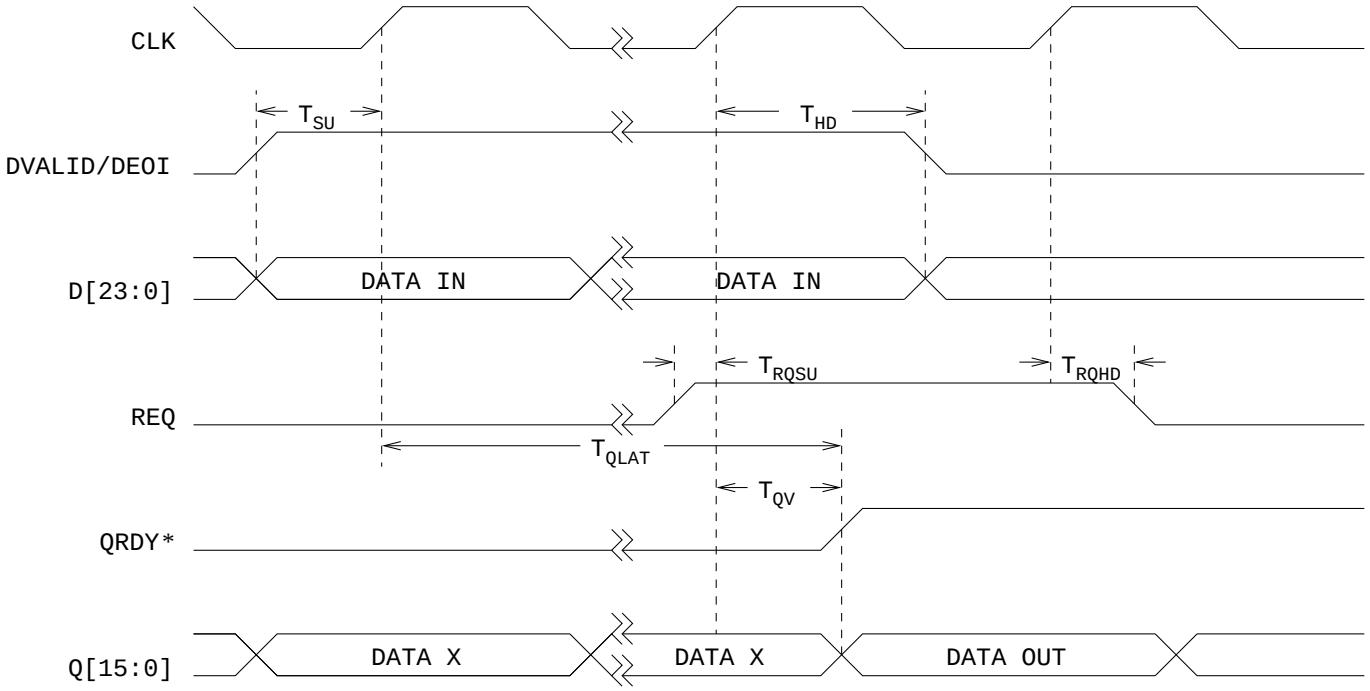
Figure 6-10: SOS and EOS Assertion

6.10 Input/Output Timing Specifications

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{SU}	Data Input Setup to CLK High	15		ns
T_{HD}	Data Input Hold after CLK High	0		ns
T_{QLAT}	Data Output Latency	note 1	note1	cycles
T_{RQSU}	REQ Setup to CLK High	15		ns
T_{QV}	Data Output Valid	5	12	ns
T_{RQHD}	REQ Hold to CLK High	0		ns

Table 6-13: Input/Output Timing

[1] See Equation 3.6.1.



* Timing for QSOS, QEOS, QRTRIG, and QFILL is same as QRDY.

Figure 6-11: Input/Output Timing

6.11 External RAM Interface Timing Specifications

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{CHSL}	CLK High to RNCSA(B) Low	5	12	ns
T_{CHWL}	CLK High to RNWEA(B) Low	7	20	ns
T_{CHDV}	CLK High to RADDA(B) and RIOA(B) Valid	5	12	ns
T_{CHWH}	CLK High to RNWEA(B) High	2	7	ns
T_{WHWL}	RNWEA(B) Pulse Width High	5	13	ns

Table 6-14: RAM Interface Write Timing

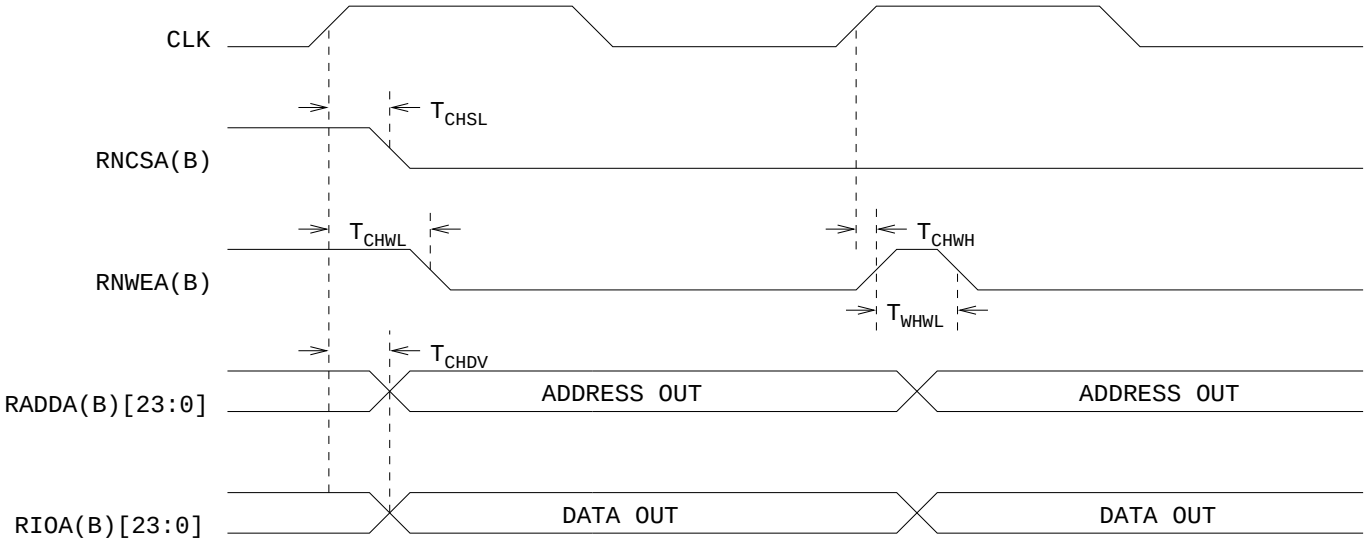


Figure 6-12: RAM Interface Write Timing

Parameter	*Description*	*Min*	*Max*	*Unit*
T_{CHGL}	CLK High to RNOEA(B) Low	5	12	ns
T_{CHQZ}	CLK High to BPE Output Float	5	12	ns
T_{CHSH}	CLK High to RNCSA(B) High	5	12	ns
T_{CHGH}	CLK High to RNOEA(B) High	5	12	ns
T_{CHQX}	CLK High to BPE Output Enable	7	16	ns

Table 6-15: RAM Interface Read Timing

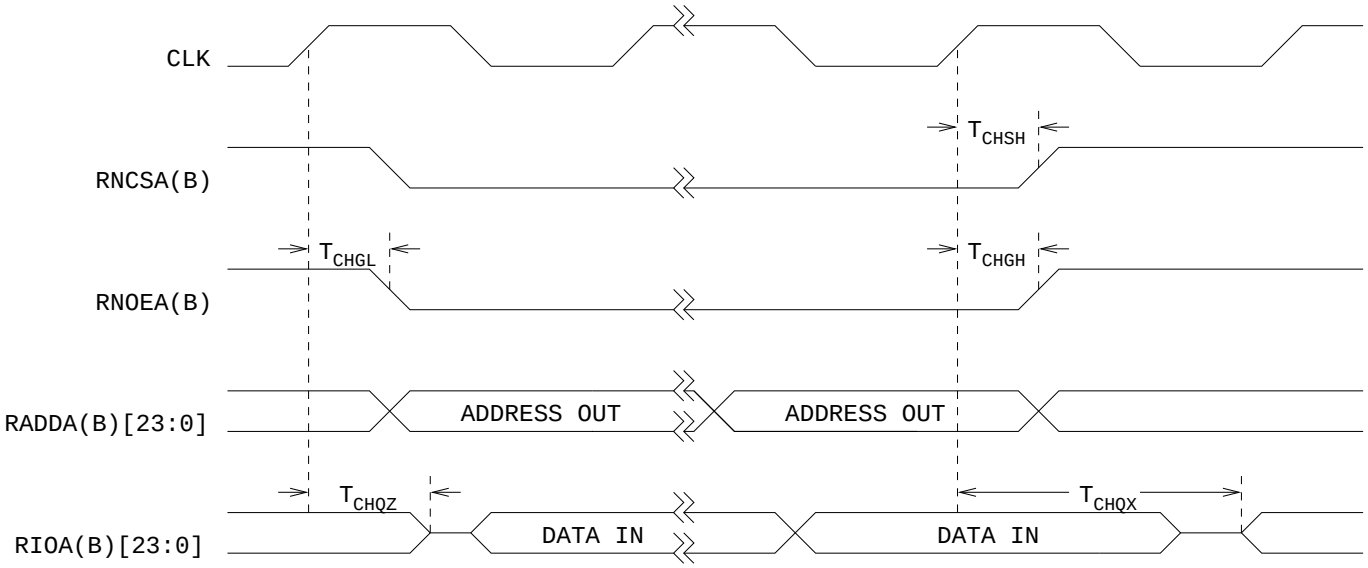


Figure 6-13: RAM Interface Read Timing

7.0 References

[1] *Image Data Compression*. Recommendation for Space Data Systems Standards. CCSDS 122.0-B-1. Blue Book. Issue 1. Washington D.C.: CCSDS, November 2005.

[2] *Image Data Compression*. Report Concerning Space Data System Standards. CCSDS 120.1-G-1. Green Book. Issue 1. Washington D.C.: CCSDS, 2007.

8.0 Appendix

8.1 Testing External RAM

To a limited extent, the BPE can be used to verify that external RAM is defect-free. However, since the BPE does not incorporate a specialized RAM test function, and because of the non-intuitive manner in which RAM data is stored under normal operating conditions, the RAM fault coverage in any devised scheme is low. Nevertheless, by sending random data to the BPE and verifying its output using a CRC function, some RAM fault coverage is possible using the following four-step method:

1. Reset the BPE according to section 3.1.
2. Using either the PINT or the SINT, pass the following parameters to the BPE:

   NB = 24, NTYPE = 2, R16 = 0,
   ROUT = 0, BPST = 0, STGST = 3, FILL = 0,
   UWTS = 1, WDC = 3, all other weights = 0,

   Set segment size (S) to a value appropriate for the RAM size. Note that segment size should not exceed the pixel capacity of the RAM as set out in Table 4-3. Also note that, given Table 4-3, segment size may have to be reduced further depending on the randomness of the data as well as its width. The wider the random input data, the fewer random blocks the BPE RAM can hold. Yet, wider input data does not always correspond to higher RAM fault coverage numbers. See Table 8-1 for a specific example involving a 128k RAM (RAM = 8).

Input Data Width[1]	**Max S**	**Approximate RAM Fault Coverage**[2]
24	400	20%
22	900	40%
20	1500	61%
16	1500	50%
8	1600	27%

Table 8-1: 128k RAM Example

[1] Recall that, according to section 4.3, any incoming data above bit-plane NB - 1 is ignored. Therefore, NB may be used to limit the incoming data width, assuming of course that the data is wider than the final value of NB. Note, also, that equation 3.4.1 still applies when setting NB.

[2] Coverage numbers assume the application of multiple, unique segments of random data.

Low fault coverage results because the BPE, when storing data in RAM, assumes compression. With random data, areas within the RAM assumed to accommodate only small amounts of data actually encounter vast amounts of data, and other areas designed with a larger capacity find themselves mostly empty. The problem of inefficient RAM storage disappears when the BPE receives compressible data. However, even with compressible data, low coverage still results since the data no longer possesses the inherent variability necessary to cover all stuck-at fault conditions.

All other BPE parameters are incidental and may be set to zero. If RAMA mode is used, RAMA mode restrictions still apply per section 3.5.

3. Using the appropriate data rate, as specified in Table 8-2, apply random data for multiple segments.

Input Data Width	Data Rate[1]
24	10Mpixels/s
20	14Mpixels/s
16	18Mpixels/s

Table 8-2: Data Rate Adjustments With Random Data

[1] Data rate assumes a clock frequency of 20MHz.

4. Verify the BPE output using a CRC function. As an aid, QVALID signals valid output data and QEOS signals the end of an output segment.

8.2 Version Control

Revision	Date	Pages	Description
1.1	December, 2010	1, 28, 29	Changed contact email. Removed no-connect (NC) annotation in Table 5-1 for the following pins: 21, 31, 41, 48, 54, 59, 73, 80, 90, 96, 100, 104, 105, 110, 112, 148, 158, 161, 168, 177, 184, 190, 202, 208, 216, 224, 231, 241, 248. Added Table 5-1 NC note.
1.2	March, 2012	1, 34	Changed contact address, phone, and email. Edited 6.3.1 to include the requirement of a rising edge on CLK.