Discrete Wavelet Transform (DWT)

SOURCE CONTROL DRAWING (SCD)

ASIC Design
Radiation Hardened

Revision – 2.1
January 27, 2011

Suggested Sources of Supply

AFX PART NUMBER	PROCURED PART NUMBER	PART MANUFACTURER	CAGE CODE
XS025A	2120327/ Discrete Wavelet Transform (DWT)	Aeroflex Colorado Springs, Inc. Colorado Springs, CO. 80907	65342

CAUTION:

THIS DEVICE IS STATIC SENSITIVE AND SHOULD BE SUBJECT TO SPECIAL HANDLING REQUIREMENTS.

Table of Contents

1.0 SCOPE

This drawing defines the requirements for the Discrete Wavelet Transform (DWT), a discrete wavelet transform radiation hardened ASIC for use in space flight applications. The part shall be manufactured and tested in accordance with the space application (also known as Class Level S) requirements of MIL-PRF-38535 by a manufacturer listed in QML-38535. The part shall have a minimum total dose radiation hardness of 50K Rad (Si).

1.1 STANDARD DEVICE TYPES

PURCHASER PART NUMBER	RELIABILITY LEVEL	REQ'D ASSEMBLY PROCESS	REQ'D SCREENING & QUALIFICATION	DIE PART NUMBER
2120327-01	Flight, Class S-Like	SECTION 3.0	SECTION 4.0	DWT XS025
2120327-02	PROTOTYPE	SECTION 3.0	SECTION 4.0	DWT XS025

2.0 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the date of request for quotation apply to the extent specified herein. In the event of a conflict between this specification and the listed documents, this specification shall govern.

Military Specifications

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for

Military Standards

MIL-STD-883	Microelectronics, Test Methods and Procedures for
MIL-STD-1580	Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts

Non-Government publications

Discrete Wavelet Transform	DWT Specification

3.0 REQUIREMENTS

3.1 General

The individual item requirements for device shall be class S-like shall be in accordance with MIL-PRF-38535 and as specified herein.

3.2 Wafer Lot

All parts delivered on any purchase order to this drawing must come from one wafer lot

3.3 Lot Date Code

Unless otherwise authorized by the purchaser in writing, all parts supplied to the requirement of this drawing on a single purchase order line item shall be from the same lot/date code shall consist of a unique, four digit minimum, numeric or alphanumeric code that represents a class S-like inspection lot.

3.4 Absolute Maximum Ratings

Absolute maximum ratings shall be as specified in Table 1, herein.

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	-65 to +150	^{o}C
T_A	Operating Temperature	-55 to +125	^{o}C
V_{VDDmax}	Max. voltage between V_{DD} and V_{SS}	-0.25 to +2.75	volts
$V_{DVDDmax}$	Max. voltage between V_{DVDD} and V_{DVSS}	-0.3 to +3.6	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DVDD}+0.3	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{DVSS}-0.3	Volts
Fmax	Maximum frequency	100	MHz

3.5 Recommended Operating Conditions:

Recommended Operating Conditions shall be as specified in Table 2, herein.

Table 2: Recommended Operating Conditions

Symbol	Parameter	Range	Units
T_A	Operating Temperature	-55 to +125	^{o}C
V_{VDD}	Standard Operating voltage V_{VDD}	2.25 to 2.75	volts
V_{DVDD}	Standard Operating voltage V_{DVDD}	3.0 to 3.6	volts

3.6 Electrical Characteristics

Electrical performance characteristics shall be as specified in Table 3, herein. The devices shall operate over the specified temperature range. AC characteristics are specified in Table 4.

3.7 Power up sequence

The VDD power must be applied either before or during of the initial application of the DVDD.

Table 3: Electrical Performance Characteristics 1/

Symbol	Parameter	Min	Max	Units	Conditions /1
VIH(min)	Min. High Level Input Voltage	0.7 * V_{DVDD}	-	volts	Guaranteed Logic '1'
VIL(max)	Max. Low Level Input Voltage	-	0.3 * V_{DVDD}	volts	Guaranteed Logic '0'
VIHC(min)	Min. High Level Input Voltage, High CLOCK Input	0.7 * V_{DVDD}	-	volts	Guaranteed Logic '1'
VILC(max)	Max. Low Level Input Voltage, Low CLOCK Input	-	0.3 * V_{DVDD}	volts	Guaranteed Logic '0'
VOH(min)	Min. High Level Output Voltage High	2.35	-	volts	IOH = -30.0 ma
VOH(min)	Min. High Level Output Voltage High	2.7	-	volts	IOH = -4.0 ma
VOL(max)	Max. Low Level Output Voltage Low	-	0.6	volts	IOH = -30.0 ma
VOL(max)	Max. Low Level Output Voltage Low	-	0.4	volts	IOH = -4.0 ma
IIH	High Level Input Leakage Current	-1	1	µA	Vin = V_{DVDD}
IIL	Low Level Input Leakage Current	-1	1	µA	Vin = V_{DVSS}
$I_{MAXQFMAX}$ 1/	Maximum quiet (core) VDD current at maximum frequency	-	1500	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Vector 8
		-	1500	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Vector 7
		-	2000	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Vector 12
		-	2000	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Vector 13
		-	4000	mA	fCLK = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Scan
$I_{MAXDFMAX}$	Maximum dirty (I/O) VDD current at maximum frequency	-	80	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Vector 8
		-	40	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Vector 7
		-	1700	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = vector 12
		-	320	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = vector 13
		-	3000	mA	f_{CLK} = 100MHz, All Pure Outputs Disconnected, All Bidirects Connected, Load = 100uA, Pattern = Scan
I_{MAXQDC}	Maximum quiet (core) VDD current at DC (no clock)	-	25	uA	T_A = -55°C , +25°C
		-	4	mA	T_A = +125°C
$I_{MAXQDCPR}$ /2	Maximum quiet (core) VDD current at DC (no clock) Post Radiation	-	150	uA	50 Krads total dose at a dose rate between 15 mrad(Si)/sec and 30 mrad(Si)/sec.
I_{MAXDDC}	Maximum dirty (I/O) VDD current at DC (no clock)	-	10	uA	T_A = -55°C , +25°C
		-	25	uA	T_A = +125°C

$I_{MAXDDCPR/2}$	Maximum dirty (I/O) VDD current at DC (no clock) Post Radiation	-	300	uA	50 Krads total dose at a dose rate between 15 mrad(Si)/sec and 30 mrad(Si)/sec.

1/: Operating Conditions: V_{DVDD} = 3.3V ± 10%, V_{DVSS} = 0V, V_{DD} = 2.5V ±10%, V_{SS} = 0V, T_A = -55°C to +125°C, unless otherwise specified.
2/ Ta = 25C

Table 4: AC Characteristics 1/

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{clkh}	CLOCK high	45%	55%	cycle	Set to 50% for testing.
t_{clkl}	CLOCK low	45%	55%	cycle	Set to 50% for testing.
t_p	CLOCK period	10		ns	f_{CLK} = 100 MHz
t_{rsth}	RESET pulse width	10		cycles	CLK cycles
t_{dsetup}	DEFAULT setup to falling edge of RST	10		cycles	CLK cycles
t_{dhold}	DEFAULT hold past falling edge of RST	1.2		cycles	CLK cycles
t_{ackh}	ACK high time	1.2		cycles	CLK cycles
t_{ackl}	ACK low time	1.2		cycles	CLK cycles
$t_{cdsetup}$	CDValid and CData setup to rising ACK	4		ns	Sweep setup time on vector set 8 to test.
t_{cdhold}	CDValid and CData hold past rising ACK	1		ns	Sweep hold time on vector set 8 to test.
$t_{bsetup\ (2)}$	BPData, BPValid and BPEOI setup to rising clock edge of DIVCLK	5		ns	
$t_{bhold\ (2)}$	BPData, BPValid and BPEOI setup to rising clock edge of DIVCLK	5		ns	
t_{sclkh}	SCLK high time	1.2		cycles	CLK cycles
t_{sclkl}	SCLK low time	1.2		cycles	CLK cycles

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{ssetup}	Sdata, SvalidN and Sreset setup to rising Sclk	4		ns	Sweep setup time on vector set 8 to test.
t_{shold}	Sdata, SvalidN and Sreset hold past rising Sclk	1		ns	Sweep hold time on vector set 8 to test.
t_{soutd} (2)	Sout delay from rising Sclk		10	ns	
t_{bpdata} (2)	CLOCK to BP* output delay	1	8	ns	Load = 50pF max.
t_{e2qd} (2)	Memory output enable (MOEN) valid low to data valid		12	ns	
t_{e2qz} (2)	Memory output enable (MOEN) valid high to data tristate		3	ns	
t_{a2qd} (2)	Memory address valid to data valid		$1.5*t_{clkp}-2$	ns	
t_{a2qh} (2)	Data valid hold time after memory address change	3		ns	
t_{wlow} (2)	memory write enable low	$1.5*t_{clkp}-2$	$1.5*t_{clkp}-2$	ns	
t_{awhold} (2)	Address hold time after rising edge of MWEN (write operation)	2		ns	
$t_{awfsetup}$ (2)	Address setup time before falling edge of MWEN	1		ns	
$t_{dwsetup}$ (2)	Data setup time before rising edge of MWEN	t_{clkp}		ns	
t_{dwhold} (2)	Data hold time after rising edge of MWEN	$0.5*t_{clkp}-2$		ns	
t_{wcycle} (2)	Write cycle time	$2*t_{clkp}-1$	$2*t_{clkp}+1$	ns	
t_{whmin} (2)	Minimum high time for MWEN between each write	$0.5*t_{clkp}-2$		ns	

1/ Operating Conditions: V_{DVDD} = 3.3V ±10%, V_{DVSS} = 0V, V_{VDD} = 2.5V ±10%, V_{SS} = 0V, T_A = -55°C to +125°C
2/ Guaranteed by simulation; testing not physically performed.

Figure 1: CLK Timing

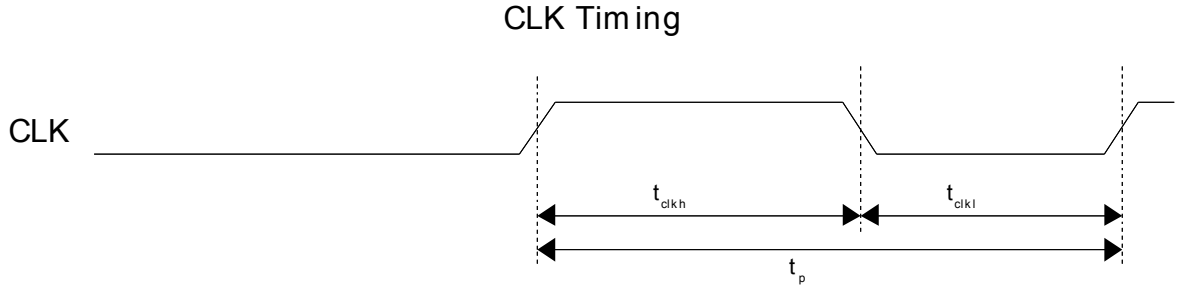


Figure 2: RST Timing

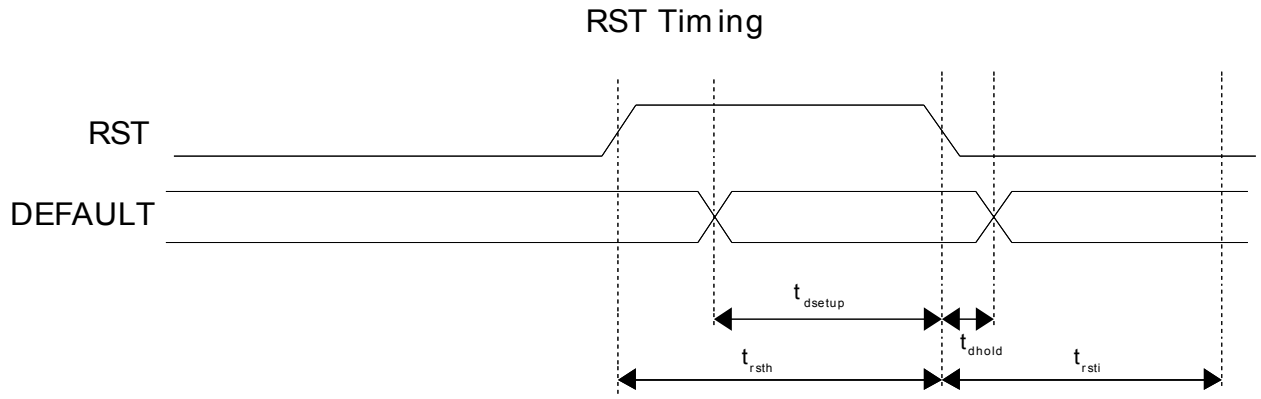


Figure 3: Memory Timing

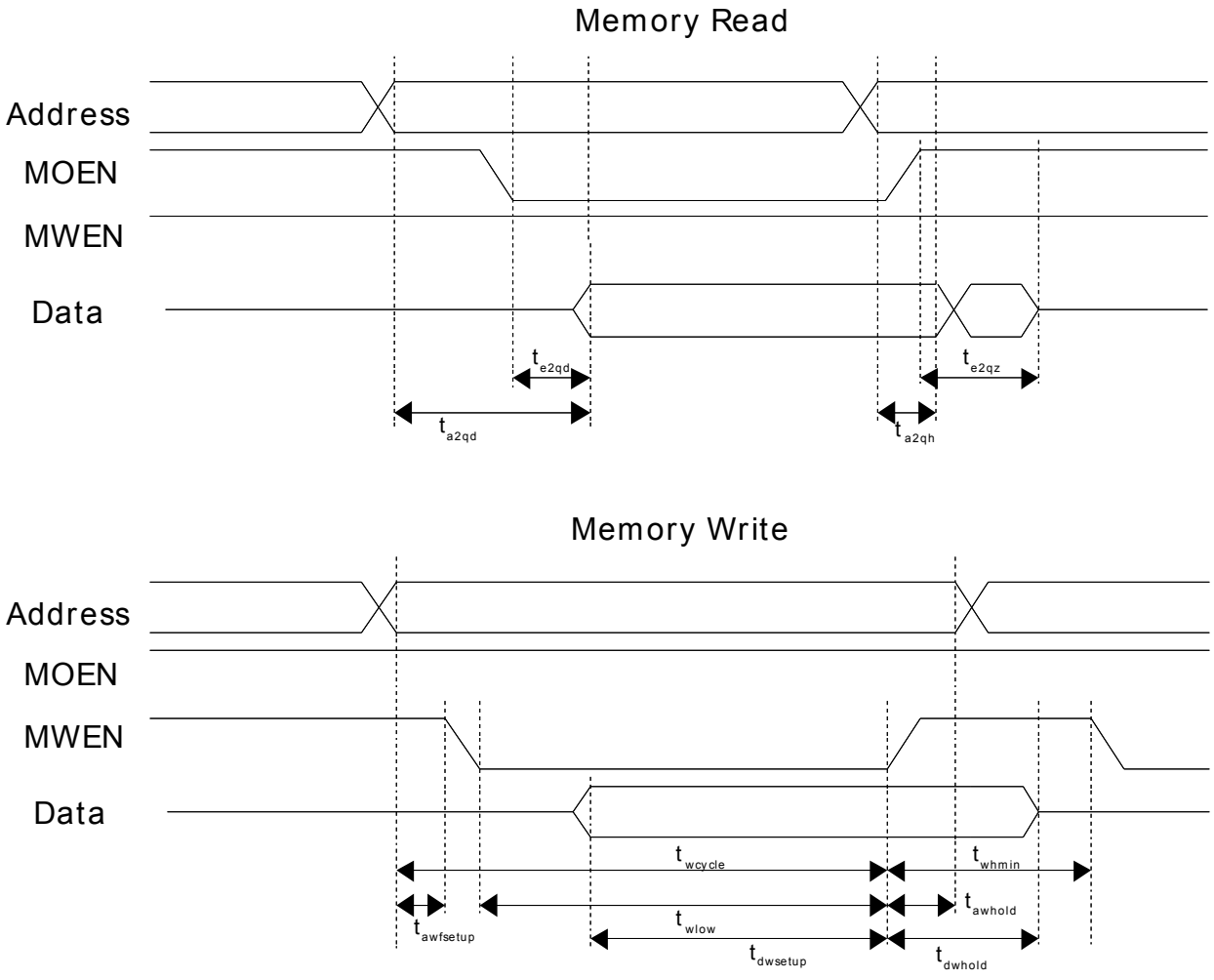


Figure 4: Data Bus Timing

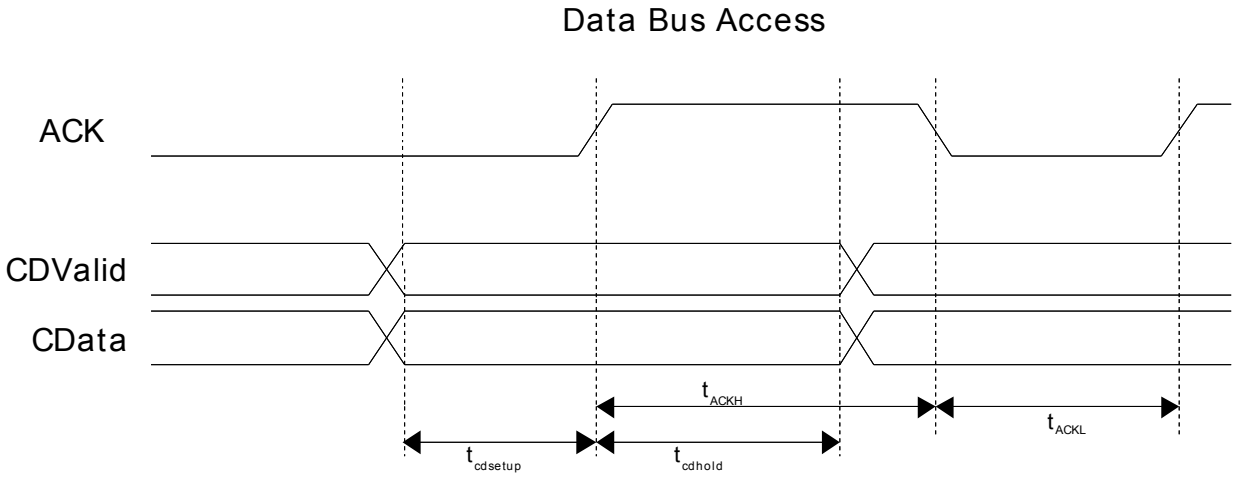


Figure 5: BPE Interface Timing

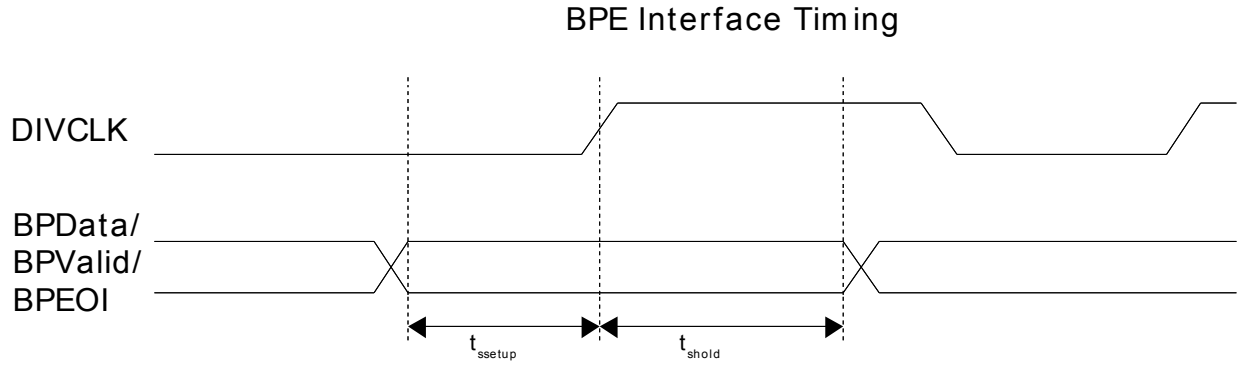
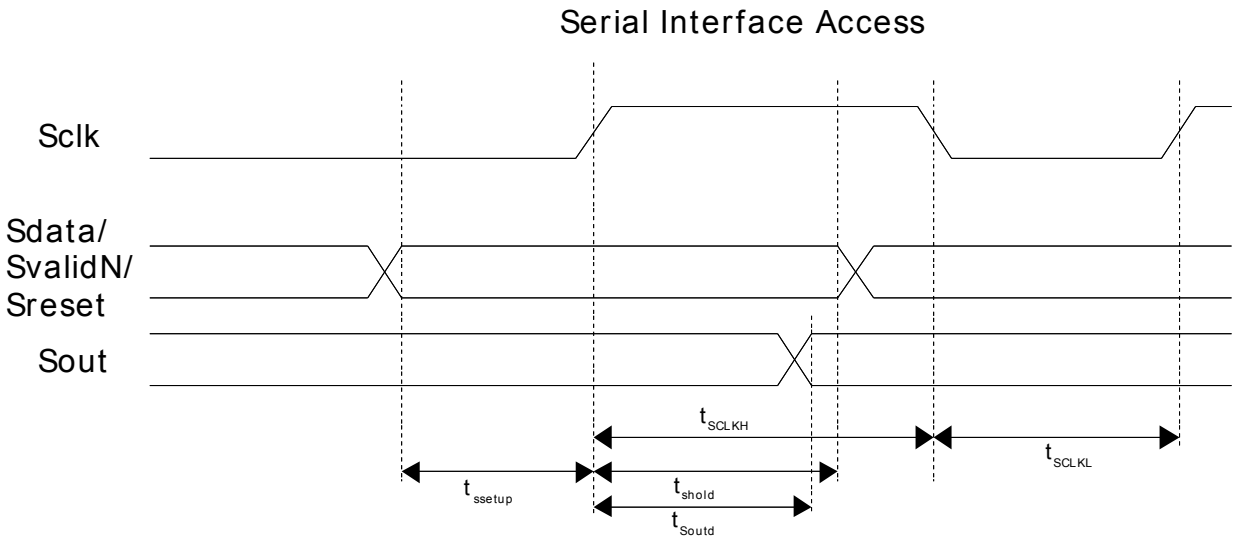


Figure 6: Serial Interface Timing



3.8 Burn-In and Life Test Circuits

The burn-in and life test duration, test condition and test temperature, Should be as specified as here in The test circuit shall specify the inputs, outputs, biases and power dissipation, as applicable, in accordance with the intent specified in MIL-STD-883, Methods 1015 and 1005. See burn-in diagram, Figure 7.

3.9 Mechanical Characteristics

3.9.1 Design, Construction, and Physical Characteristics

In accordance with Table 9 and Figure 8.

3.10 Marking

In accordance with MIL-PRF-38535 and the following:

3.10.1 Part Marking Requirement, Class Level S-like

2120327-001(2)
ARXX (3) DWT_XS025 (4)
USA (5) YYWWA (6)
Δ(1) YYWW (7) 0ABCA (8)
XXX (9)

(1) Pin 1 indicator and ESD identifier
(2) Customer part number
(3) Aeroflex trademark, Name, or Symbol
(4) Aeroflex part identification code
(5) Country of origin
(6) Inspection lot code
YYWW = Inspection lot code
A = Inspection sublot(s)
(7) Seal week
YY = Last two digits of the year the assembly lot was sealed
WW = The work week that the assembly lot was sealed
(8) Assembly Lot number
(9) Serial number

3.10.2 Part Marking Requirement, Prototype

Proto(6)
2120327-002(2)
ARXX (3) DWT_XS025A (4)
USA (5) YYWW (7)
Δ(1) 0ABCA (8)

(1) Pin 1 indicator and ESD identifier
(2) Customer part number
(3) Aeroflex trademark, Name, or Symbol
(4) Aeroflex part identification code
(5) Country of origin
(6) Device type
(7) Seal week
YY = Last two digits of the year the assembly lot was sealed
WW = The work week that the assembly lot was sealed
(8) Assembly Lot number

3.11 Serialization

When specified in the purchase order, prior to the first recorded electrical measurement in screening, each microcircuit shall be marked with a unique serial number assigned consecutively within the level of the individual microcircuit within that inspection lot.

3.12 Radiation Hardness Assurance

When tested as specified in Appendix B and C of MIL-PRF-38535 and in accordance with Method 1019 Condition C of MIL-STD-883, the part shall meet a total ionization radiation dose of 50K Rad(Si), RHA level L.

3.12.1 Traceability

Inspection lot records shall be maintained to provide traceability from the device serial number to the specific wafer lot or to the specific wafer when testing to any Group E subgroup is performed on a wafer by wafer basis.

3.12.2 RLAT and LATCH-UP Testing.

Validation complete by CAMBR laboratory testing to 100Krad min. Latch up testing passed to LET 120 Mev cm2 / mg .

3.13 Environmental Testing

The device shall meet the requirements of this drawing following exposure to any singular or natural combination of the environmental conditions specified in the quality assurance provisions of this document.

3.14 Workmanship

The devices shall be processed in such a manner as to be uniform in quality and shall be free from any defects that would adversely affect life, serviceability or appearance.

3.15 Wafer Lot Acceptance

ICs LLC OF McCALL IDAHO Is Source of Wafers/Dice. Recommended Manufacturing Foundry Shall be TSMC-WAFERTECH LLC, CAMAS, WA. . The wafer lot shipped for Assembly processes should be accompanied by a copy of Certification Of Conformance. The wafer lot should be 1st optical inspected and wafer probed as the wafer lot acceptance of receipt prior to Assembly processes.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Prototype Screening

Prototype devices will be processed per manufacturer's standard prototype flow. Additional requirements if any shall be documented in the purchase order.

4.2 Sampling and inspection

Sampling and inspection procedures shall be in accordance with Table 5.

4.3 Screening

Screening shall be in accordance with Table 5, and shall be conducted on all devices prior to qualification and technology conformance inspection.

Table 5: Lot Screening Flow

Screen	Class Level S-Like Method
Wafer Lot Acceptance	---
Non-Destructive Bond Pull	2023; In-line SPC alternative
Precap Visual	2010, Cond A
Temperature Cycling	1010 Cond C
Constant Acceleration	2001
Particle Impact Noise Detection (PIND)	2020, Cond A
Seal Test (Fine / Gross Leak)	1014
Radiography	2012
Pre Burn-in Electrical	Applicable specification
Dynamic Burn-in	1015
Interim Electrical Test	Applicable specification
Percent Defective Allowable (PDA)	PDA 5%, 3% for Functional
Final Electrical Test	Applicable specification
External Visual Inspection	2009

4.4 Qualification inspection

Qualification inspection shall be in accordance with the source control drawing..
Inspections to be performed shall be group A, group C, package first article evaluation and group E inspections (see 4.4.1 through 4.4.4).

TABLE 6: Electrical Test Requirements

Test requirements	Subgroups (in accordance with MIL-PRF-38535, Table 3)
Interim electrical parameters (see 4.3)	- - -
Final electrical parameters (see 4.3)	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7 add 2,3,8,9,10 & 11
Group D end-point electrical parameters (see 4.4)	1, 7
Group E end-point electrical parameters (see 4.4)	- - -

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection

Per MIL-STD-883, Test Method 5005, in-line alternative

4.4.2 Group C Inspection

The group C inspection end-point electrical parameters shall be as specified in table 6 herein. The steady-state life test duration, test condition and test temperature shall be in accordance with test method 1005 of MIL-STD-883. or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883. Group C sample size is 12 parts.

4.4.3 4.4.3 Group D inspection.

The group D package test will be performed as first article functional evaluation test. A 16 piece sample will be subjected to a simulated package assembly flow and will be subjected to 40 temperature cycles, centrifuge, and fine & gross leak test before being submitted to the test listed in the following table:

Table 7: Package First Article Functional Evaluation

Evaluation /Test	Test conditions	Sample plan	Criteria / Notes
Thermal Series Evaluation	Per M5005, D-3 15 Thermal Shocks 100 Temperature cycles Fine/Gross leak test	15/0	Per Mil-Std-883, M5005, D-3 test requirements
Salt Atmosphere	Per M1009, Cond A	15/0	Visual Inspection per M1009
Physical Dimensions	Per M2016	2/0	Per Package drawing
Solderability	Per M2003	22/0 Sample 22 leads from 3 devices	Solder temperature 245˚C +/- 5˚C

4.4.4 Group E Inspection

Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.13 herein). RHA levels for device class S-Like shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table 6 herein.

4.4.5 Total Dose Irradiation Testing

Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition C. Sample size is 5 parts and taken from Group C samples after completion of group C testing. The Group E testing will be performed at a dose rate between 15 mrads(Si)/sec and 30mrad(Si)/sec to a total dose of 50 Krad (Si).

4.5 Destructive Physical Analysis

DPA will be performed by NASA.

4.6 Failure Analysis

Catastrophic failures (i.e. shorts or opens measurable or detectable at 25°C) subsequent to burn-in shall be analyzed. Reporting of failure and documentation of the analysis shall be in accordance with the provisions of the purchase order.

4.7 Inspection Verification

The customer reserves the right to witness testing, as specified in the procurement document, and prior to shipment will verify that all requirements of the purchase order and this specification have been satisfied.

4.7.1 Customer Source Inspection

When source inspection is specified in the procurement document, the supplier shall notify the customer's procuring agent FIVE days in advance of shipment so that appropriate planning can be made. The supplier shall make available in-process manufacturing, acceptance tests and other related documentation for the microcircuit lot submitted for final inspection for acceptance. Pre Cap source inspection is required.

4.8 Deliverable Data Items

The supplier's standard Class S-Like data package shall be delivered with the devices under procurement for the inspection lot and as a minimum consist of the following:

a. 100% lot screening summary with in-line Group A.
b. Radiography report.
c. Group C report (wafer lot specific).
d. Package First Article Functional Evaluation report
e. Group E data as applicable
f. Variable data for pre-burn-in 25˚C and post-burn-in electrical tests (25˚C , 125˚C and -55˚C).
g. Variable data for post life test electrical tests (25˚C , 125˚C and -55˚C).
h. Certificate of Conformance
i. Failure Analysis Report, if applicable.

4.8.1 Correlation of Parts and Data Items

Parts delivered in each shipment shall be identified (e.g., individual unit packaging, tagging, or sticker affixed to part) so that data is identifiable to the individual parts contained in the shipment.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging

In accordance with MIL-PRF-38535.

5.2 Package Marking

The first level protective package shall be marked with the device part number, lot date code, serial number[s] and supplier name or identification. Higher level packaging shall include the above marking plus the purchase order number. The purchase order number must appear on the outermost package.

5.3 Special Handling Labels

Special handling labels shall be affixed to the exterior of the shipping containers to indicate that the contents are ESD sensitive.

6.0 ORDERING INFORMATION

As applicable, Customer Procurement Documents shall specify the following:

- This document and revision number
- Additions, deletions, and exceptions to this document
- Microcircuit Part Number
- DPA Requirements
- Failure Analysis Report
- Customer Source Inspection Requirements

Table 9: Device Pin-out

PIN	FUNCTION	I/O TYPE
1	VDD	
2	VSS	
3	NC	
4	NC	
5	NC	
6	NC	
7	NC	
8	NC	
9	NC	
10	NC	
11	NC	
12	NC	
13	BP_5	CMOS Output
14	BP_4	CMOS Output
15	BP_3	CMOS Output
16	BP_2	CMOS Output
17	BP_1	CMOS Output
18	BP_0	CMOS Output
19	BP_VLD	CMOS Output
20	BP_EOI	CMOS Output
21	D1_23	CMOS IN-OUT
22	DVDD	
23	DVSS	
24	D1_22	CMOS IN-OUT
25	D1_21	CMOS IN-OUT
26	D1_20	CMOS IN-OUT
27	D1_19	CMOS IN-OUT
	D1_18	CMOS IN-OUT

PIN	FUNCTION	I/O TYPE
28		
29	D1_17	CMOS IN-OUT
30	D1_16	CMOS IN-OUT
31	D1_15	CMOS IN-OUT
32	D1_14	CMOS IN-OUT
33	D1_13	CMOS IN-OUT
34	D1_12	CMOS IN-OUT
35	D1_11	CMOS IN-OUT
36	D1_10	CMOS IN-OUT
37	D1_9	CMOS IN-OUT
38	D1_8	CMOS IN-OUT
39	D1_7	CMOS IN-OUT
40	D1_6	CMOS IN-OUT
41	D1_5	CMOS IN-OUT
42	VDD	
43	VSS	
44	D1_4	CMOS IN-OUT
45	D1_3	CMOS IN-OUT
46	D1_2	CMOS IN-OUT
47	D1_1	CMOS IN-OUT
48	D1_0	CMOS IN-OUT
49	MEM_18	CMOS Output
50	MEM_17	CMOS Output
51	TESTEN	CMOS Input
52	SCANEN	CMOS Input
53	OSC_EN	CMOS Input
54	NC	
55	NC	

PIN	FUNCTION	I/O TYPE
56	NC	
57	NC	
58	NC	
59	NC	
60	NC	
61	NC	
62	NC	
63	DVDD	
64	DVSS	
65	VDD	
66	VSS	
67	NC	
68	NC	
69	NC	
70	NC	
71	NC	
72	NC	
73	NC	
74	NC	
75	NC	
76	NC	
77	NC	
78	NC	
79	NC	
80	NC	
81	OSCOUT	CMOS Output
82	MEM_16	CMOS Output
83	MEM_15	CMOS Output
84	MEM_14	CMOS Output
	MEM_13	CMOS Output

PIN	FUNCTION	I/O TYPE
85		
86	DVDD	
87	DVSS	
88	MEM_12	CMOS Output
89	MEM_11	CMOS Output
90	MEM_10	CMOS Output
91	MEM_9	CMOS Output
92	MEM_8	CMOS Output
93	MEM_7	CMOS Output
94	MEM_6	CMOS Output
95	MEM_5	CMOS Output
96	MEM_4	CMOS Output
97	MEM_3	CMOS Output
98	MEM_2	CMOS Output
99	MEM_1	CMOS Output
100	MEM_0	CMOS Output
101	MWEN	CMOS Output
102	ADDR_B	CMOS Output
103	ADDR_A	CMOS Output
104	MOEN	CMOS Output
105	D0_23	CMOS IN-OUT
106	VDD	
107	VSS	
108	D0_22	CMOS IN-OUT
109	D0_21	CMOS IN-OUT
110	D0_20	CMOS IN-OUT
111	D0_19	CMOS IN-OUT
112	D0_18	CMOS IN-OUT
113	D0_17	CMOS IN-OUT
114	NC	

PIN	FUNCTION	I/O TYPE
115	NC	
116	NC	
117	NC	
118	NC	
119	NC	
120	NC	
121	NC	
122	NC	
123	NC	
124	NC	
125	NC	
126	NC	
127	DVDD	
128	DVSS	
129	VDD	
130	VSS	
131	NC	
132	NC	
133	NC	
134	NC	
135	NC	
136	NC	
137	NC	
138	NC	
139	NC	
140	D0_16	CMOS IN-OUT
141	D0_15	CMOS IN-OUT
142	D0_14	CMOS IN-OUT
143	D0_13	CMOS IN-OUT
	D0_12	CMOS IN-OUT

PIN	FUNCTION	I/O TYPE
144		
145	D0_11	CMOS IN-OUT
146	D0_10	CMOS IN-OUT
147	D0_9	CMOS IN-OUT
148	D0_8	CMOS IN-OUT
149	D0_7	CMOS IN-OUT
150	DVDD	
151	DVSS	
152	D0_6	CMOS IN-OUT
153	D0_5	CMOS IN-OUT
154	D0_4	CMOS IN-OUT
155	D0_3	CMOS IN-OUT
156	D0_2	CMOS IN-OUT
157	D0_1	CMOS IN-OUT
158	D0_0	CMOS IN-OUT
159	CLK	CMOS Input
160	RST	CMOS Input
161	NOBND	
162	SCLK	CMOS Input
163	SRST	CMOS Input
164	SDATA	CMOS Input
165	SVLDN	CMOS Input
166	SOUT	CMOS Output
167	DCLK	CMOS Output
168	DCLK2	CMOS Output
169	ERR	CMOS Output
170	VDD	
171	VSS	
172	HFULL	CMOS Output
173	CD_15	CMOS Input

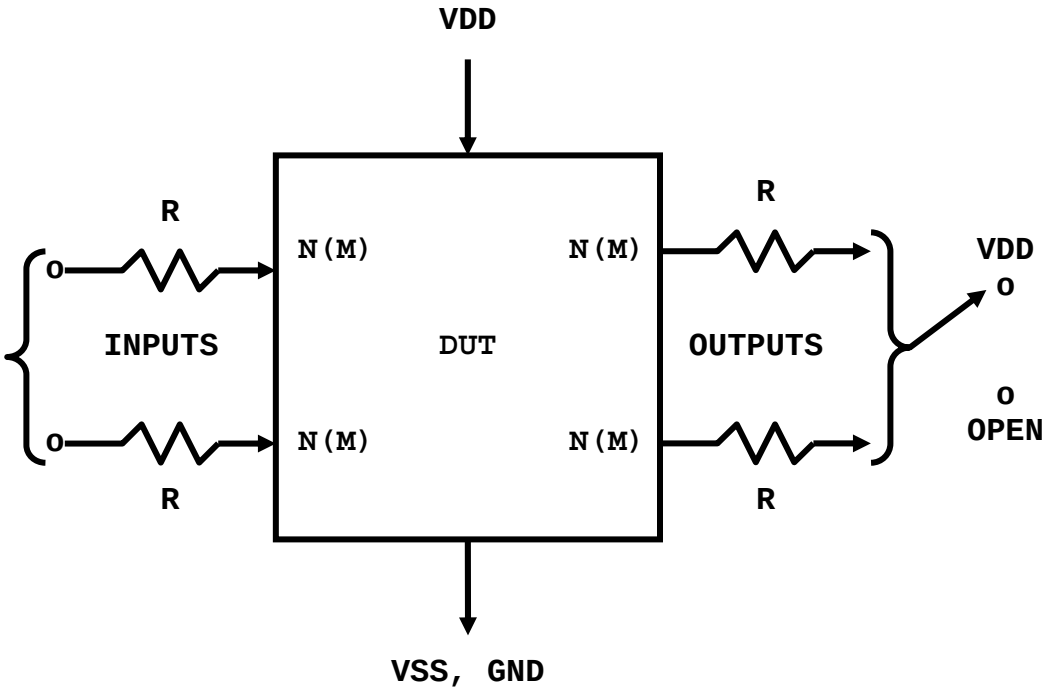
PIN	FUNCTION	I/O TYPE
174	CD_14	CMOS Input
175	CD_13	CMOS Input
176	CD_12	CMOS Input
177	CD_11	CMOS Input
178	CD_10	CMOS Input
179	CD_9	CMOS Input
180	CD_8	CMOS Input
181	CD_7	CMOS Input
182	NC	
183	NC	
184	NC	
185	NC	
186	NC	
187	NC	
188	NC	
189	NC	
190	NC	
191	DVDD	
192	DVSS	
193	VDD	
194	VSS	
195	NC	
196	NC	
197	NC	
198	NC	
199	NC	
200	NC	
201	NC	
202	NC	
	NC	

PIN	FUNCTION	I/O TYPE
203		
204	NC	
205	NC	
206	NC	
207	NC	
208	CD_6	CMOS Input
209	CD_5	CMOS Input
210	CD_4	CMOS Input
211	CD_3	CMOS Input
212	CD_2	CMOS Input
213	CD_1	CMOS Input
214	DVDD	
215	DVSS	
216	CD_0	CMOS Input
217	ACK	CMOS Input
218	CD_VLD	CMOS Input
219	FLSH	CMOS Input
220	DFT	CMOS Input
221	TREEEN	CMOS Input
222	BP_23	CMOS Output
223	BP_22	CMOS Output
224	BP_21	CMOS Output
225	BP_20	CMOS Output
226	BP_19	CMOS Output
227	BP_18	CMOS Output
228	BP_17	CMOS Output
229	BP_16	CMOS Output
230	BP_15	CMOS Output
231	BP_14	CMOS Output
232	BP_13	CMOS Output

PIN	FUNCTION	I/O TYPE
233	BP_12	CMOS Output
234	VDD	
235	VSS	
236	BP_11	CMOS Output
237	BP_10	CMOS Output
238	BP_9	CMOS Output
239	BP_8	CMOS Output
240	BP_7	CMOS Output
241	BP_6	CMOS Output
242	NC	
243	NC	
244	NC	
	NC	

PIN	FUNCTION	I/O TYPE
245		
246	NC	
247	NC	
248	NC	
249	NC	
250	NC	
251	NC	
252	NC	
253	NC	
254	NC	
255	DVDD	
256	DVSS	

Figure 7: Burn-In Diagrams



Notes:

1. For Dynamic Burn-in, all inputs shall be connected through resistors to CP (Clock Pulse). Inputs that have pull up or pull down resistors may be connected to CP, VDD or Gnd. Outputs shall be open or connected through resistors to VDD. Bidirects shall be connected through resistors to VDD. R = 2.49K ohms ±10% resistor to reflect a 2mA minimum load condition.
2. CP = 100KHz ±15%; duty cycle = 50% ±15%; VIH = 2.5V to VDD; VIL = 0 ±.5V; transitions time < 0.5uS. An alternative (CP) or vector pattern may be applied to input pins depending on burn-in chamber limitations.
3. VDD(VCC) = Minimum, depending on oven capability, Maximum, depending on wafer process. (Typ: 3.6V – 8.0V) Limits and specifications also apply to any multiple voltage supplies.
4. I = input, O = output, T = three state output, PU = pull-up, PD = pull-down, B(I/O) = bidirect, N(M) = highest numbered inputs, bidirect, output, etc. as stated.

Figure 8: Package Outline Drawing – units in mm