| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add case outline “Y”. - tmh | 99-04-01 | Monica L. Poelking |
| B | Add case outline “Z”. Update boileplate. -phn | 01-06-27 | Thomas M. Hess |
| C | Add footnote 2/ to 1.2.4 for case outline ‘Z’ . Add paragraph 3.3.2.1 to the AID requirements. -phn | 01-12-12 | Thomas M. Hess |

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | B | B | B | B | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | | | | | | | | | | | | | | | | |

| REV STATUS OF SHEETS | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | C | B | C | B | C | B | | A | | | | B | B | B | | |
| SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | |

PMIC N/A

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DRAWING APPROVAL DATE
97-12-02

REVISION LEVEL
**C**

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43216**
**http://www.dscc.dla.mil**

# STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, CUSTOM ASIC, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| **A** | **67268** | **5962-97B04** |

SHEET 1 OF 18

DSCC FORM 2233
APR 97

5962-E129-02

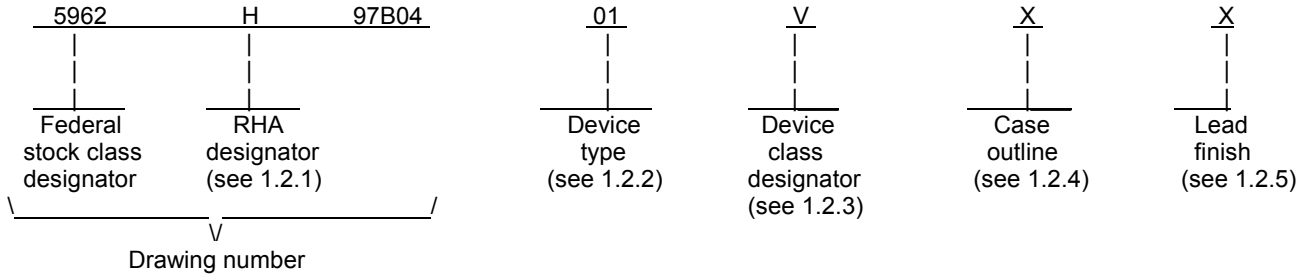
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN) in the applicable Altered Item Drawing (AID). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

Customizations (personalizations) for each design, including circuit organization, electrical performance characteristics, and test conditions, shall be specified in an Altered Item Drawing (AID) (see 3.3 herein).

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Circuit (total number of usable gates) | Array family |
|---|---|---|
| 01 | <5,000 usable gates | UT25E/R |
| 02 | 10,000 usable gates | UT25E/R |
| 03 | 15,000 usable gates | UT25E/R |
| 04 | 20,000 usable gates | UT25E/R |
| 05 | 25,000 usable gates | UT25E/R |
| 06 | 35,000 usable gates | UT35E/R |
| 07 | 75,000 usable gates | UT75E/R |
| 08 | 125,000 usable gates | UT100E/R |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style 1/ | $\theta_{JC}$ Thermal resistance |
|---|---|---|---|---|
| X | See figure 1 | 64 | Flatpack | 3/ |
| Y | CMGA15-P84 | 84 | Pin grid array | 3/ |
| Z | See figure 1 2/ | 84 | Flatpack | 3/ |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 4/

Supply voltage range ($V_{DD}$) ..... -0.3 V dc to +7.0 V dc
Voltage at any pin range ($V_{I/O}$) ..... -0.3 V dc to $V_{DD}$ + 0.3 V dc
Power dissipation ($P_D$) ..... as specified in the AID.
Storage temperature range ($T_{STG}$) ..... -65°C to +150°C
Lead temperature (soldering, 5 seconds) ..... +300°C
Latch-up immunity ($I_{LU}$) ..... ±150 mA
DC input current ($I_I$) ..... ±10 mA
Junction temperature ($T_J$) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range ($V_{DD}$) ..... +4.5 V dc to +5.5 V dc
Operating temperature range ($T_C$) ..... -55°C to +125°C
DC input voltage range ($V_{IN}$) ..... 0 V dc to $V_{DD}$

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) ..... As specified in the AID

1.6 Radiation features
Total dose (dose rate = 50 – 300 rad(Si)/s) ..... $1.0 \times 10^6$ rads(Si) 5/
Dose rate upset
01 - 06 ..... $5.0 \times 10^9$ rads(Si)/sec 6/
07, 08 ..... $1.0 \times 10^9$ rads(Si)/sec 6/
Dose rate survivability
01 - 06 ..... $1.0 \times 10^{13}$ rads(Si)/sec 7/
07, 08 ..... $1.0 \times 10^{12}$ rads(Si)/sec 7/
SIngle event upset ..... $< 1.0 \times 10^{-10}$ errors per cell-day 7/ 8/
Linear energy threshold ..... $\leq$ 36 MeV/(mg/cm$^2$)
LET no upsets ..... See 4.4.4.4
Neutron fluence ..... $1.0 \times 10^{14}$ n/cm$^2$
Latchup ..... Latchup immune over maximum operating conditions

1/ Additional packages are available in SMD 5962-96B02.
2/ Unless otherwise specified in the AID, the pin 1 identifier will be as shown in figure 1.
3/ As specified in the AID.
4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
5/ Total dose Co-60 testing in accordance with MIL-STD-883, method 1019.
6/ Short pulse 20 ns FWHM (full width, half maximum).
7/ May be design dependent.
8/ SEU-hard flip-flop cell. Non-hard flip-flop cell is $5 \times 10^{-8}$ errors per cell-day.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, bulletin, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.1.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issures are those cited in the solicitation.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Radiation exposure circuit. The radiation exposure circuit shall be as specified in figure 2.

3.3 AID requirements. All AIDs written against this SMD shall be sent to DSCC-VA. The following items shall be provided to the device manufacturer by the customer as part of an AID. Items 3.3.3 through 3.3.9 form a part of the manufacturer's design database/database archive. These items shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. As such, these items will not appear in the AID in the traditional sense.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.2.1 Case outline "Z": Unless otherwise specified in the AID, the pin 1 identifier will be as shown in figure 1.

3.3.3 Functional block diagram (or equivalent VHDL behavioral description). 9/

3.3.4 Logic diagram ( or equivalent structural VHDL description). 9/

3.3.5 Pin function description.

3.3.6 Design tape # or design document name (i.e., net list).

3.3.7 Design functional tape # or name.

3.3.8 Test functional tape # or name.

3.3.9 Switching waveform(s).

3.3.10 Fault coverage. The extent of fault coverage is controlled by the quality of the customers design input, therefore fault coverage shall be specified by the customer.

3.3.11 Device electrical performance characteristics. Device electrical performance characteristics shall include dc parametric (see table I herein for minimum requirements), functional, input to output ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended ambient operating temperature range and specified test load conditions.

3.3.12 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.13 Radiation hardness assurance. Additional radiation hardness requirements shall be specified in the AID.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID number shall be added to the marking by the manufacturer.

9/ If VHDL is utilized for documentation, a VHDL test bench shall be included for both behavioral and structural VHDL descriptions. Behavioral VHDL descriptions shall include function and timing at the port accurate enough to perform test generation and determine fault detection/fault isolation levels at the integrated circuits pins when performing board or subsystem simulations. For guidelines see DI-EGDS-80811.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output voltage low 3/ | $V_{OL1}$ | $V_{DD}$ = 4.5 V, $I_{OL}$ = 2.0 mA | 1,2,3 | All | | 0.4 | V |
| | $V_{OL2}$ | $I_{OL}$ = 4.0 mA | 1,2,3 | All | | 0.4 | |
| | $V_{OL3}$ | $I_{OL}$ = 8.0 mA | 1,2,3 | All | | 0.4 | |
| | $V_{OL4}$ | $I_{OL}$ = 12.0 mA | 1,2,3 | All | | 0.4 | |
| | $V_{OL5}$ | $I_{OL}$ = 1.0 µA | 1,2,3 | All | | 0.05 | |
| | $V_{OL6}$ | $I_{OL}$ = 100 µA | 1,2,3 | All | | 0.25 | |
| | $V_{OL7}$ | $I_{OL}$ = 100 µA | 1,2,3 | All | | 1.0 | |
| Output voltage high 3/ | $V_{OH1}$ | $V_{DD}$ = 4.5 V, $I_{OH}$ = -2.0 mA | 1,2,3 | All | 2.4 | | |
| | $V_{OH2}$ | $I_{OH}$ = -4.0 mA | 1,2,3 | All | 2.4 | | |
| | $V_{OH3}$ | $I_{OH}$ = -8.0 mA | 1,2,3 | All | 2.4 | | |
| | $V_{OH4}$ | $I_{OH}$ = -12.0 mA | 1,2,3 | All | 2.4 | | |
| | $V_{OH5}$ | $I_{OH}$ = -1.0 µA | 1,2,3 | All | $V_{DD}$-0.05 V | | |
| | $V_{OH6}$ | $I_{OH}$ = -100 µA | 1,2,3 | All | $V_{DD}$-0.25 V | | |
| | $V_{OH7}$ | $I_{OH}$ = -100 µA | 1,2,3 | All | 3.5 | | |
| Input leakage current 4/ | $I_{IN1}$ | $V_{IN} = V_{DD}$ or $V_{SS}$ | 1,2,3 | All | -1 | +1 | µA |
| | $I_{IN2}$ | $V_{IN} = V_{DD}$ | 1,2,3 | All | +150 | +900 | |
| | $I_{IN3}$ | $V_{IN} = V_{SS}$ | 1,2,3 | All | -10 | +10 | |
| | $I_{IN4}$ | $V_{IN} = V_{SS}$ | 1,2,3 | All | -900 | -150 | |
| | $I_{IN5}$ | $V_{IN} = V_{DD}$ | 1,2,3 | All | -10 | +10 | |
| Output leakage current 5/ | $I_{OZ1}$ | $V_O = V_{DD}$ and $V_{SS}$ | 1,2,3 | All | -5 | +5 | |
| | $I_{OZ2}$ | | 1,2,3 | All | -10 | +10 | |
| | $I_{OZ3}$ | | 1,2,3 | All | -20 | +20 | |
| | $I_{OZ4}$ | | 1,2,3 | All | -30 | +30 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output current short-circuit 5/ 6/ | $I_{OS1}$ | $V_O = V_{DD}$ and $V_{SS}$ | 1,2,3 | All | -50 | +50 | mA |
| | $I_{OS2}$ | | 1,2,3 | All | -100 | +100 | |
| | $I_{OS3}$ | | 1,2,3 | All | -200 | +200 | |
| | $I_{OS4}$ | | 1,2,3 | All | -300 | +300 | |
| Quiescent supply current | $I_{DDQ}$ | $V_{DD}$ = 5.5 V | 1,2,3 | All | | 1 | mA |
| | | M, D, P, L, R, F, G, H | | | | 4 | |
| Schmitt Trigger | $V_{T+}$ | | 1,2,3 | All | | 4 | V |
| | $V_{T-}$ | | 1,2,3 | All | 1 | | |
| Hysteresis range 6/ | $V_{TH}$ | | 1,2,3 | All | 1.5 | 2 | |
| Low level input voltage 7/ | $V_{IL}$ | TTL inputs | 1,2,3 | All | | 0.8 | |
| | | CMOS, OSC inputs | | | | $0.3*V_{DD}$ | |
| High level input voltage 7/ | $V_{IH}$ | TTL inputs | 1,2,3 | All | 2.2 | | |
| | | CMOS, OSC inputs | | | $0.7*V_{DD}$ | | |
| Input capacitance | $C_I$ | $V_{DD}$ = Open<br>f = 1 MHz<br>See 4.4.1c | 4 | All | | 15 | pF |
| Output capacitance 5/ | $C_{O1}$ | | 4 | All | | 15 | |
| | $C_{O2}$ | | 4 | All | | 15 | |
| | $C_{O3}$ | | 4 | All | | 17 | |
| | $C_{O4}$ | | 4 | All | | 25 | |
| Bidirect input/output capacitance 8/ | $C_{IO1}$ | | 4 | All | | 16 | |
| | $C_{IO2}$ | | 4 | All | | 20 | |
| | $C_{IO3}$ | | 4 | All | | 26 | |
| Functional tests 9/ | | $V_{DD}$ = 5.5 V and 4.5 V<br>See 4.4.1b | 7,8 | All | | | |

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ Devices supplied to this drawing will meet all levels M, D, P, L, R, F, G and H of irradiation. However, this device is only tested at the 'H' level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C.
2/ 4.5 V dc < $V_{DD}$ < 5.5 V dc, -55°C < $T_C$ < 125°C, inputs are driven with $V_{IL}$ maximum and $V_{IH}$ minimum as specified in table I unless otherwise specified.
3/ $V_{OL1}$ and $V_{OH1}$ = TTL half-drive buffer.
$V_{OL2}$ and $V_{OH2}$ = TTL single-drive buffer.
$V_{OL3}$ and $V_{OH3}$ = TTL double-drive buffer.
$V_{OL4}$ and $V_{OH4}$ = TTL triple-drive buffer.
$V_{OL5}$ and $V_{OH5}$ = CMOS outputs.
$V_{OL6}$ and $V_{OH6}$ = CMOS outputs (optional).
$V_{OL7}$ and $V_{OH7}$ = OSC outputs.
4/ $I_{IN1}$ = TTL CMOS, and Schmitt inputs.
$I_{IN2}$ = inputs with pull-down resistors.
$I_{IN3}$ = inputs with pull-down resistors, OSC.
$I_{IN4}$ = inputs with pull-up resistors.
$I_{IN5}$ = inputs with pull-up resistors, OSC.
5/ $I_{OZ1}$, $I_{OS1}$, and $C_{01}$ = TTL half-drive buffer.
$I_{OZ2}$, $I_{OS2}$, and $C_{02}$ = TTL single-drive, CMOS, OSC buffer.
$I_{OZ3}$, $I_{OS3}$, and $C_{03}$ = TTL double-drive buffer.
$I_{OZ4}$, $I_{OS4}$, and $C_{04}$ = TTL triple-drive buffer.
6/ Supplied as a design limit but not guaranteed or tested.
7/ $V_{IL}$ and $V_{IH}$ threshold levels are verified by performance of a low switching noise functional test or a dc $V_{IL}/V_{IH}$ NAND-TREE test pattern.
8/ $C_{IO1}$ = TTL single-drive, CMOS, OSC buffer.
$C_{IO2}$ = TTL double-drive buffer.
$C_{IO3}$ = TTL triple-drive buffer.
9/ Functional tests are conducted in accordance with MIL-STD-883, method 5004 with the following input test conditions: $V_{IH}$ = $V_{IH}$(min) +20%, -0%; $V_{IL}$ = $V_{IL}$(max) =0%, -50% as specified herein for TTL and CMOS compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}$(min) and $V_{IL}$(max).

TABLE IB. SEP test limits . 1/ 2/

| Device type | $T_A$ = Temperature ± 10°C 3/ | $V_{CC}$ = 4.5 V | | Bias for latch-up test $V_{CC}$ = 5.5 V no latch-up LET = 3/ |
|---|---|---|---|---|
| | | Effective LET no upsets [MEV/(mg/cm$^2$)] | Maximum device cross section ($\mu m^2$) (LET = 120) | |
| All | +25°C | 4/ | 4/ | 4/ |

**NOTES: Devices that contain cross coupled resistance must be tested at the maximum rated $T_A$.**

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature $T_A$ = +125°C.
4/ When characterized as a result of the procuring activities request, this parameter will be specified.

Case X

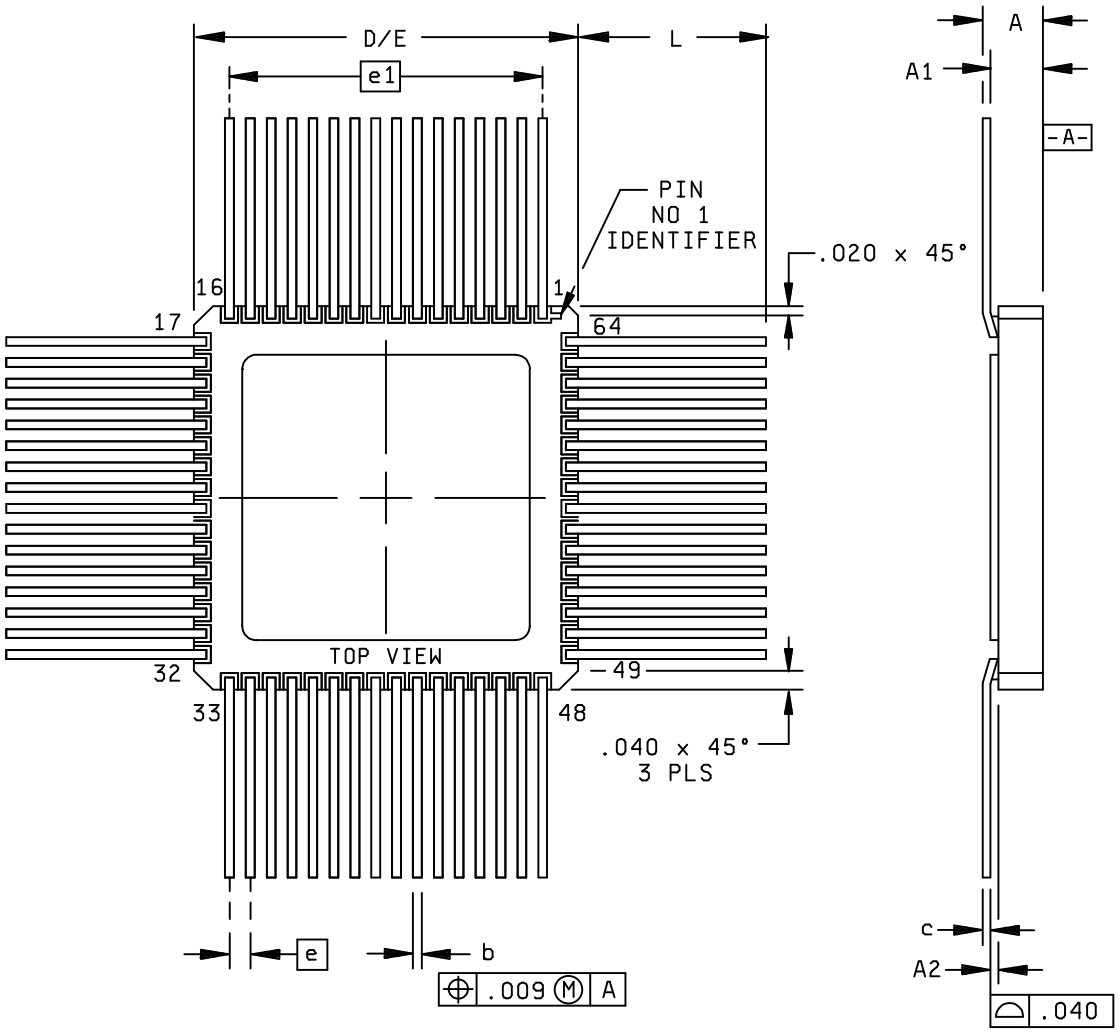



FIGURE 1. Case outline.

| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 | SIZE A | | 5962-97B04 |
|---|---|---|---|
| | | REVISION LEVEL | SHEET 10 |

Case X

| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 2.286 | 2.794 | 0.090 | 0.110 |
| A1 | 1.829 | 2.235 | 0.072 | 0.088 |
| A2 | | 0.305 | | 0.012 |
| b | 0.356 | 0.457 | 0.014 | 0.018 |
| c | 0.178 | 0.254 | 0.007 | 0.010 |
| D/E | 22.606 | 23.114 | 0.890 | 0.910 |
| e | 1.270 BSC | | 0.050 BSC | |
| e1 | 19.050 BSC | | 0.750 BSC | |
| L | 6.350 | | 0.250 | |

NOTES:
1. All exposed metalized areas are gold plated over nickel plating.
2. The lid is electrically connected to VSS.

FIGURE 1. Case outline - Continued.

Case Z

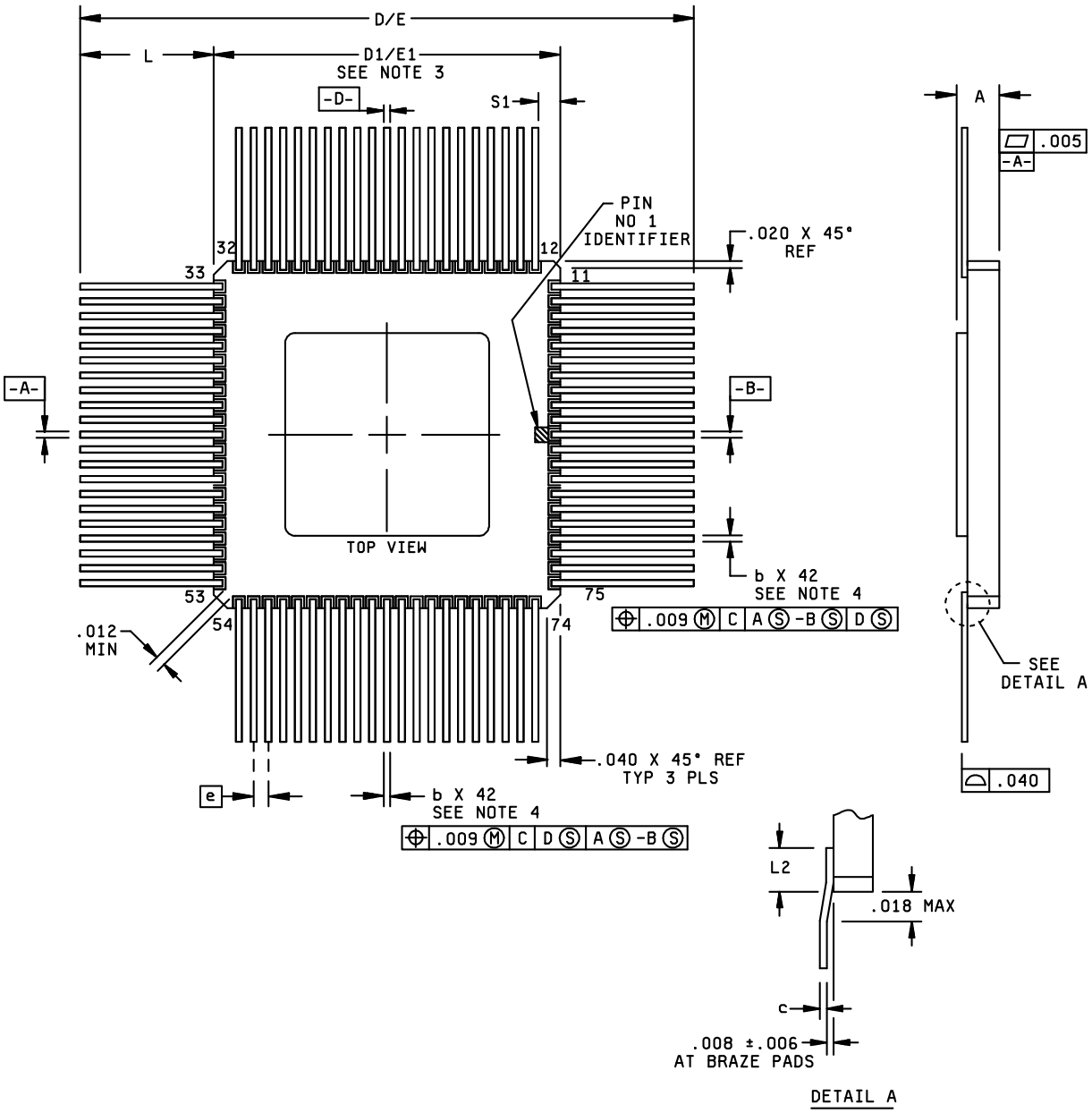



FIGURE 1. Case outline - Continued.

Case Z

| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 2.032 | 2.743 | 0.080 | 0.108 |
| b | 0.356 | 0.457 | 0.014 | 0.018 |
| c | 0.152 | 0.203 | 0.006 | 0.008 |
| D/E | 45.593 | 46.355 | 1.795 | 1.825 |
| D1/E1 | 28.905 | 29.515 | 1.138 | 1.162 |
| e | 1.270 BSC | | 0.050 BSC | |
| L2 | 0.635 | | 0.025 | |
| S1 | 0.127 | | 0.005 | |

NOTES:
1. All exposed metalized areas are gold plated over nickel plating.
2. The lid is electrically connected to VSS.
3. Maximum envelope for ceramic is 1.175 inches square. This includes ceramic mismatch and tolerances, ceramic and braze infections, and runout.
4. All leads increase maximum limit by 0.003 inches measured at the center of the flat, when lead finish a (solder) is applied.

FIGURE 1. Case outline - Continued.

| Open | $V_{DD}$ = 5 V ± 0.5 V | GND |
|---|---|---|
| A2-A8, A10, A12, A13, A15-A18, B2-B4, B6-B13, B15, B16, B18, C6-C17, D2, D6-D12, D17, E1, E7-E9, F1-F3, F14, F16-F18, G1-G5, G14-G18, H1-H4, H14-H18, J2-J4, J14, J15, J17, J18, K1-K4, K17, L2-L4, L15-L17, M1-M4, M15-M18, N1-N3, N15-N18, P3, P7, P17, P18, R2, R7-R12, R17, R18, T7-T15, T18, U6-U17, V4-V7, V9, V11, V12, V14, V15 | A1, A9, A11, B1, B17, C1-C3, C18, D1, D3, D16, D18, E4, E15, E18, F4, F5, F15, H5, J1, J5, K15, K16, K18, L1, L5, L14, L18, M5, M14, N5, N14, P2, P4, P6, P8-P10, P12, P13, P16, R1, R3-R6, R14-R16, T1-T5, U1-U4, V1-V3, V8, V10, V17, V18 | A14, B5, B17, C5, D13, E2, E3, E10, E12, E16, E17, J16, N4, P1, P15, R13, T6, T16, T17, U5, U18, V13, V16 |
| $V_{DD}$ External Pin | GND External | |
| F8, F10, F12, G6, H13, J6, K13, L6, M13, N7, N9, N11 | F7, F9, F11, G13, H6, J13, K6, L13, M6, N8, N10, N12 | |

NOTES:
1. Each pin except F7, F8, F10, F11, F12, G6, G13, H6, H13, J6, J13, K6, K13, L6, L13, M6, M13, N7, N8, N9, N10, N11, and N12 will have a resistor of 2.49K Ω ∀ 5% for irradiation.
2. The irradiation circuit provided is for the standard evaluation circuit. This package can be found on SMD 5962-96B02 case outline W.

FIGURE 2. Radiation exposure circuit

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 ($C_I$, $C_O$, and $C_{IO}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | | | 1, 7 |
| Final electrical parameters (see 4.2) | 1, 2, 3, 7, 8, 9, 10, 11 1/ | 1, 2, 3, 7, 8, 9, 10, 11 1/ | 1, 2, 3, 7, 8, 9, 10, 11 2/ |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

TABLE IIB. Delta limits

| Parameter | Condition | LImits |
|---|---|---|
| $I_{DDQ}$ | $T_A$ = 25°C | ±10% of measured value or 35 μA whichever is greater |

NOTE: If device is tested at or below 35 μA no deltas are required. Delta's are performed at room temperature.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-PRF-38535 and MIL-STD-883 method 1019, (condition A ) and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IB herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (See 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be as required in MIL-PRF-38535. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60E to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm$^2$.

c. The flux shall be between $10^2$ and $10^5$ ions/cm$^2$/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 01-12-12

Approved sources of supply for SMD 5962-97B04 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard Microcircuit Drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962H97B0401QXC | 65342 | UT25E/R_QCH |
| 5962H97B0401VXC | 65342 | UT25E/R_VCH |
| 5962H97B0402QXC | 65342 | UT25E/R_QCH |
| 5962H97B0402VXC | 65342 | UT25E/R_VCH |
| 5962H97B0402QYA | 65342 | UT25E/R_QCH |
| 5962H97B0402VYA | 65342 | UT25E/R_VCH |
| 5962H97B0402QZA | 65342 | UT25E/R_QCH |
| 5962H97B0402VZA | 65342 | UT25E/R_VCH |
| 5962H97B0402QZC | 65342 | UT25E/R_QCH |
| 5962H97B0402VZC | 65342 | UT25E/R_VCH |
| 5962H97B0403QXC | 65342 | UT25E/R_QCH |
| 5962H97B0403VXC | 65342 | UT25E/R_VCH |
| 5962H97B0404QXC | 65342 | UT25E/R_QCH |
| 5962H97B0404VXC | 65342 | UT25E/R_VCH |
| 5962H97B0405QXC | 65342 | UT25E/R_QCH |
| 5962H97B0405VXC | 65342 | UT25E/R_VCH |
| 5962H97B0406QXC | 65342 | UT35E/R_QCH |
| 5962H97B0406VXC | 65342 | UT35E/R_VCH |
| 5962H97B0407QXC | 65342 | UT75E/R_QCH |
| 5962H97B0407VXC | 65342 | UT75E/R_VCH |
| 5962H97B0408QXC | 65342 | UT100E/R_QCH |
| 5962H97B0408VXC | 65342 | UT100E/R_VCH |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 65342 | Aeroflex UTMC Microelectronic Systems<br>4350 Centennial Boulevard<br>Colorado Springs, CO 80907-3486 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.