Space Qualified High Speed Reed Solomon Encoder t=16

Product Specification

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November 3, 2005 - address change only

Features:

- (N,N-32) Reed Solomon encoder
- Code specified by CCSDS standard
- 200 Mbits/sec sustained output data rate
- Pin selectable interleaving depth (I=1-8)
- No special clocks required
- Sub-micron (leff) silicon gate CMOS fabrication
- Radiation-hardened to $3X10^6$ rads (Si) total dose
- LET threshold $>$ 40 MeV-cm^2/mg
- SEU-hardened to less than $1.0X10^{-10}$ errors/bit-day

1 General Description

This chip implements a Reed Solomon (RS) encoder. An RS code is a powerful cyclic symbol error correcting code. This code is useful in obtaining correct data through a burst error channel and thus has potential applications in communication systems and in digital systems where burst error conditions could exist. Under normal operation, the code is a (255,223) code. Due to the flexible nature of the algorithms being implemented, the circuit will support the encoding of shortened, as well as full length RS codes. Specifically, the codes which are supported are of the form: $(255-i,223-i)$, where i can be any integer from 0 to 222.

The code is defined over the finite field $GF(2^8)$. The field defining primitive polynomial is $p(x) = x^8 + x^7 + x^2 + x^1 + x^0$ and the generator polynomial is given by:

$$G(x) = \prod_{i=112}^{143} (x - \beta^i)$$

where $\beta = \alpha^{11}$. The encoder represents data in the Dual Basis defined by the following transforms:

$$[z_0, z_1, \ldots, z_7] = [u_7, u_6, \ldots, u_0] \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$[u_7, u_6, \ldots, u_0] = [z_0, z_1, \ldots, z_7] \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 \end{bmatrix}$$

where $[z_0, z_1, \ldots, z_7]$ is the symbol represented by the dual basis and $[u_7, u_6, \ldots, u_0]$ is the symbol represented by the normal basis.

The coder circuit has data input and output ports. Data is input at a constant rate, and output with a fixed latency. The latency of the encoder is one clock. Data is input in a byte serial fashion and with only one clock delay, is output byte serial. After the information bytes have been output, the next 32 output bytes are the RS check bytes. The output data rate for the chip is 200 Mbits/sec when clocked at a rate of 25 MHz.

The encoder can be programmed to interleave the data at depths of one, two, ... or eight. Interleaving of two or more encoded messages allows higher burst error correction capabilities. The interleaving depth, I, is controlled by external pins, S_0, S_1 and S_2.

2 Circuit Operation

2.1 Initialization

Before proper circuit operation can begin, an encoder section must be initialized and the interleave depth chosen. This is accomplished by bringing the reset input (RST) high for at least two clock pulses and setting the interleave depth control lines, S_0, S_1 and S_2, to the appropriate state.

S_2	S_1	S_0	I
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

At this time, it is also necessary to bring the input control (INC) inactive low to ensure no spurious messages are processed. Two clock pulses after RST is brought low, circuit operation may commence. The circuit may be re-initialized at any time but any messages being processed by the encoder section at that time will be lost. Zeros are clocked into the parity generator whenever INC is low.

2.2 Encoder Operation

Assuming the above initialization sequence has been performed, encoding is performed in the following manner. INC is brought high coincidentally with the first message symbol to be encoded. It remains

high while successive message symbols are clocked into the encoder on the data input bus (DI). Symbols are clocked in and out of the circuit on the rising edge of the symbol clock (CK).

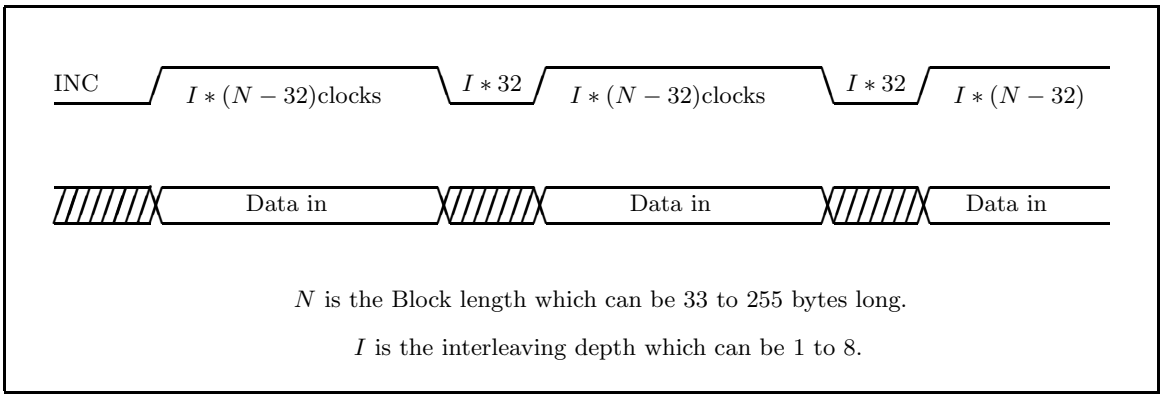

Figure 1: Timing Diagram for the INC signal.

INC is brought low again when the last message symbol has been clocked into the circuit. It must remain low at least $32I$ clock cycles, during which time the parity symbols will be clocked out of the circuit. This operation also fills the parity generator with zeros. If INC is held low longer than $32I$ clock cycles, zeros will appear on the the data output bus (DO). Bringing INC high after it has been low for $32I$ or more clock cycles starts the processing of the next message. The timing for INC is shown in Figure 1.

2.3 Bypass Operation

After a reset operation or after a block has been encoded and the parity read from the chip, a data bypass operation can occur. Data can flow through the encoder without being encoded by bringing the bypass input control (BIC) high coincidentally with the first byte of data to be passed unprocessed by the chip. After the one clock cycle latency, the data entering on DI appears on DO and continues to pass through the chip as long as BIC remains high. While BIC is high, INC should be held low to keep the registers in the parity generator held reset.

2.4 Space Enhancement Features

The CMOS fabrication process used is reported to be tolerant of total dose radiation levels exceeding 1 Mrad. In addition, the chip is designed to provide protection against Single Event Upsets (SEU) in two ways. First, the process and gate array cells are reported to be hardened against errors to less than $1.0X10^{-10}$ errors/bit-day. Second, the control structure and data path are configured to completely reset after each message insuring that an SEU of the data registers will effect at most one encoded message.

3 System Outputs

The delay through the encoder is one clock cycle. Thus, one clock cycle after INC is brought high, the output control (OUTC) goes high specifying the start of a valid code word. When OUTC goes low, the encoder is outputting the check symbols. An overall timing diagram for the encoder is shown in Figure 2.

The data inputs and outputs of the encoder are TTL compatible.

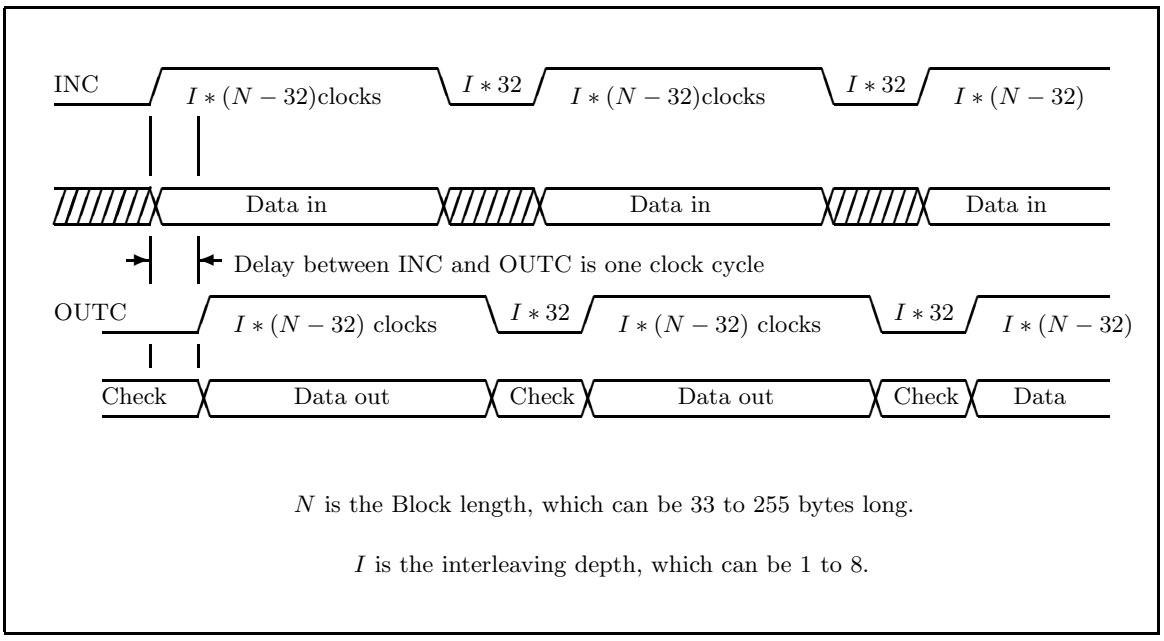

Figure 2: Overall timing diagram for the encoder.

4 Block Diagram

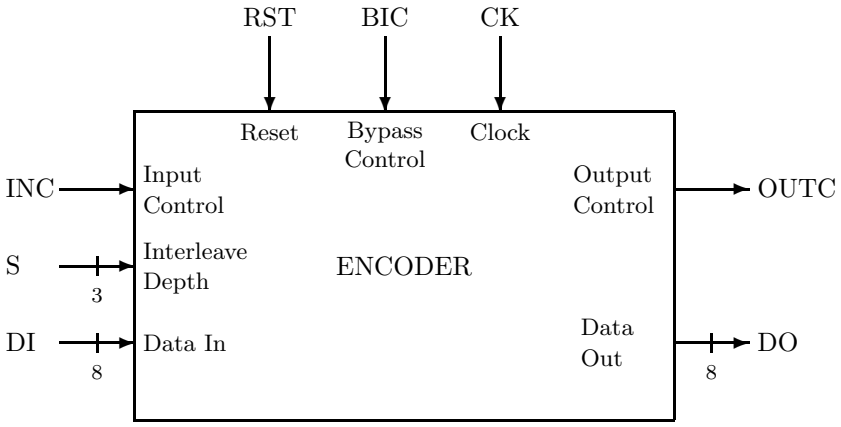

Figure 3: Block Diagram for the Encoder.

5 Pin Description

Pin Number	Name	Function
12,22,32,53,64,73	V_{DD}	Power Supply, normally +5V
1,11,31,43,52,74	V_{SS}	Ground Reference
18	RST	Reset input
19	BIC	Bypass Control
20	INC	Data Input Control
76	OUTC	Control Output
16	S_0	Interleave Control LSB
15	S_1	Interleave Control
14	S_2	Interleave Control MSB
8	CK	Symbol Clock input
23	DI_0	1st bit of input data bus (LSB)
24	DI_1	2nd bit of input data bus
25	DI_2	3rd bit of input data bus
26	DI_3	4th bit of input data bus
27	DI_4	5th bit of input data bus
28	DI_5	6th bit of input data bus
29	DI_6	7th bit of input data bus
30	DI_7	8th bit of input data bus (MSB)
84	DO_0	1st bit of output data bus (LSB)
83	DO_1	2nd bit of output data bus
82	DO_2	3rd bit of output data bus
81	DO_3	4th bit of output data bus
80	DO_4	5th bit of output data bus
79	DO_5	6th bit of output data bus
78	DO_6	7th bit of output data bus
77	DO_7	8th bit of output data bus (MSB)
63	DC_TEST	Input threshold test output

6 Pin Configuration

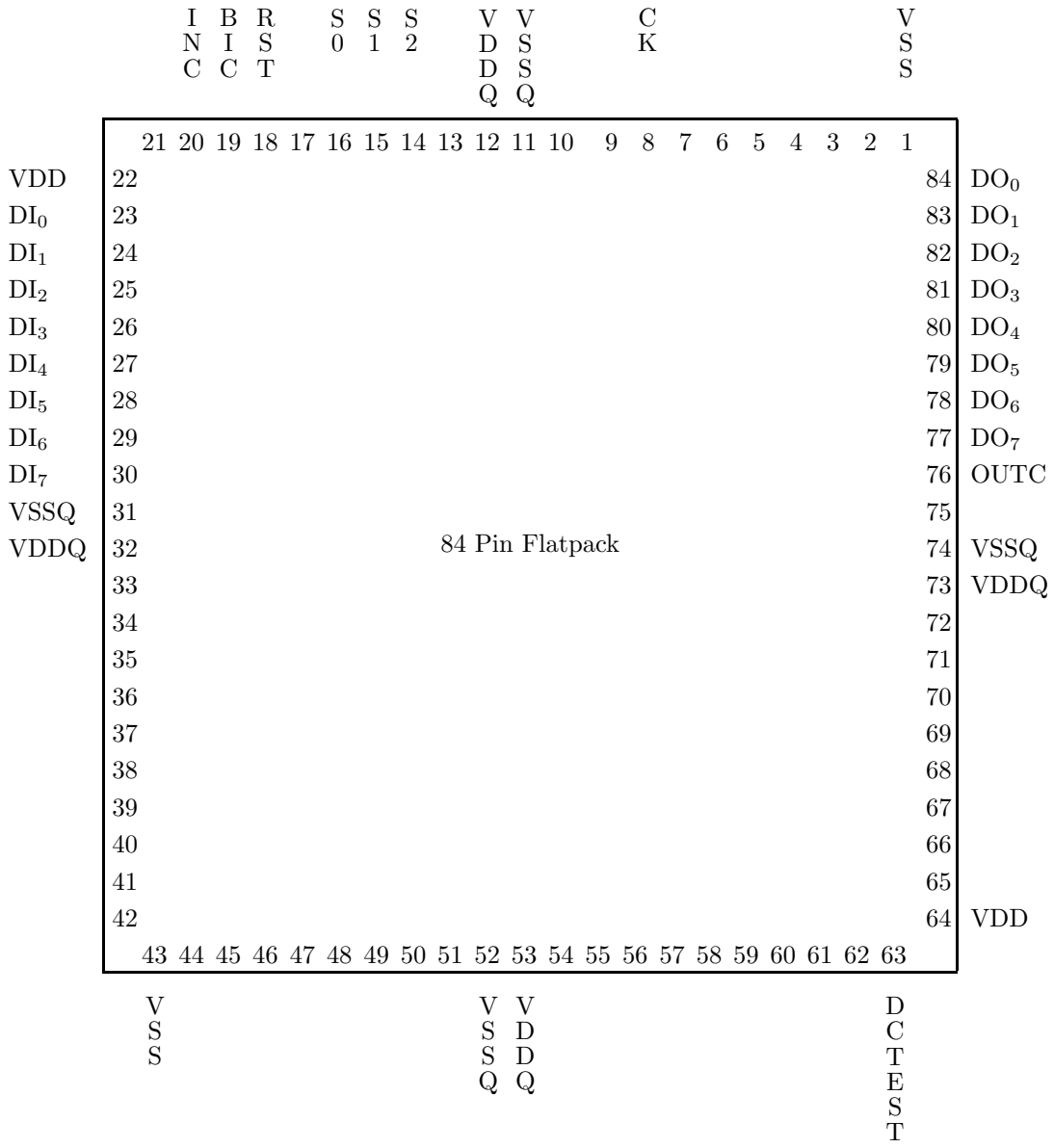

Figure 4: Pin configuration

7 Signal Descriptions

7.1 Control Inputs

CK Clock is the master clock.

RST Reset, active HIGH. RST initializes the registers in the parity generator. The signal must be held high at least two clock cycle. Data input may begin after RST is returned inactive (low) for at least two clock cycles.

INC Input control, active HIGH. INC frames the input message bytes and defines block length. The signal is brought high coincidentally with the first byte of data and is brought low after the last data byte.

BIC Bypass control, active HIGH. BIC frames input bytes that should pass through the encoder without being encoded. The signal is brought high coincidentally with the first byte of data and is brought low after the last data byte.

S_x Interleaving Select lines control the interleaving depth, with $S_2S_1S_0$ of (000) being an interleave of one, (001) an interleave of two, ... and (111) an interleave of eight. These lines must be stable before leaving reset prior to entering data after a power up sequence or a change in the interleaving depth.

7.2 Control Outputs

OUTC Output Control, active HIGH. OUTC signals when the message bytes are output. The signal is INC delayed by the chip latency (one clock cycle).

7.3 Data Inputs/Outputs

DI_{0-7} Data Inputs. Bit 7 is the most significant bit.

DO_{0-7} Data Outputs. Bit 7 is the most significant bit.

8 Electrical Specifications: Reference is ground (Vss)

Absolute Maximum Ratings					
Symbol	Parameter	Min.	Max.	Unit	
V_{DD}	Supply Voltage	-0.3	7	V	
V_I	Voltage at Digital Inputs	-0.3	$V_{DD} + 0.3$	V	
I_I	Current at Digital Inputs		± 10	mA	
V_O	Voltage at Digital Outputs	-0.3	$V_{DD} + 0.3$	V	
I_O	Current at Digital Outputs		± 10	mA	
$T_{STORAGE}$	Storage Temperature	-65	150	°C	

Recommended Operating Conditions					
Symbol	Characteristics	Min.	Max.	Unit	
V_{DD}	Supply Voltage	4.5	5.5	V	
T_{OP}	Operating Temperature	-55	125	°C	
V_I	Input Voltage	0	V_{DD}	V	

DC Electrical Characteristics					
Symbol	Characteristics	Min.	Max.	Units	Test Conditions
V_{IH}	Input High Voltage	2.2		V	
V_{IL}	Input Low Voltage		0.8	V	
I_{IL}	Input Leakage		1	μA	
V_{OH}	Output High Voltage	2.4	V_{DD}	V	$I_{OH} = -4.0$mA
V_{OL}	Output Low Voltage	V_{SS}	0.4	V	$I_{OL} = 4.0$mA
I_{OH}	Output High Current	4.0		mA	Source; $V_{OH} = 2.4$V
I_{OL}	Output Low Current		4.0	mA	Sink; $V_{OL} = 0.4$V
PD	Encoder Power Dissipation		70	mW/MHz	CL = 50pF

AC Electrical Characteristics					
Symbol	Parameter	Min.	Max.	Units	Test Conditions
tck	Clock Cycle Time	40		ns	Note 1
tckr	Clock Rise Time		2	ns	Note 2
tckf	Clock Fall Time		2	ns	Note 3
tckw	Clock Pulse Width	16		ns	Note 4
tisu	Input Set Up	6		ns	Note 5
tih	Input Hold	1		ns	Note 6
tsd	Output Delay		24	ns	CL = 50pF

Notes:

1. Measured from valid Vil to valid Vil.
2. Measured from valid Vil to valid Vih.
3. Measured from valid Vih to valid Vil.
4. Measured from valid Vih to valid Vih.
5. Includes INC control input.
6. Includes INC control input.

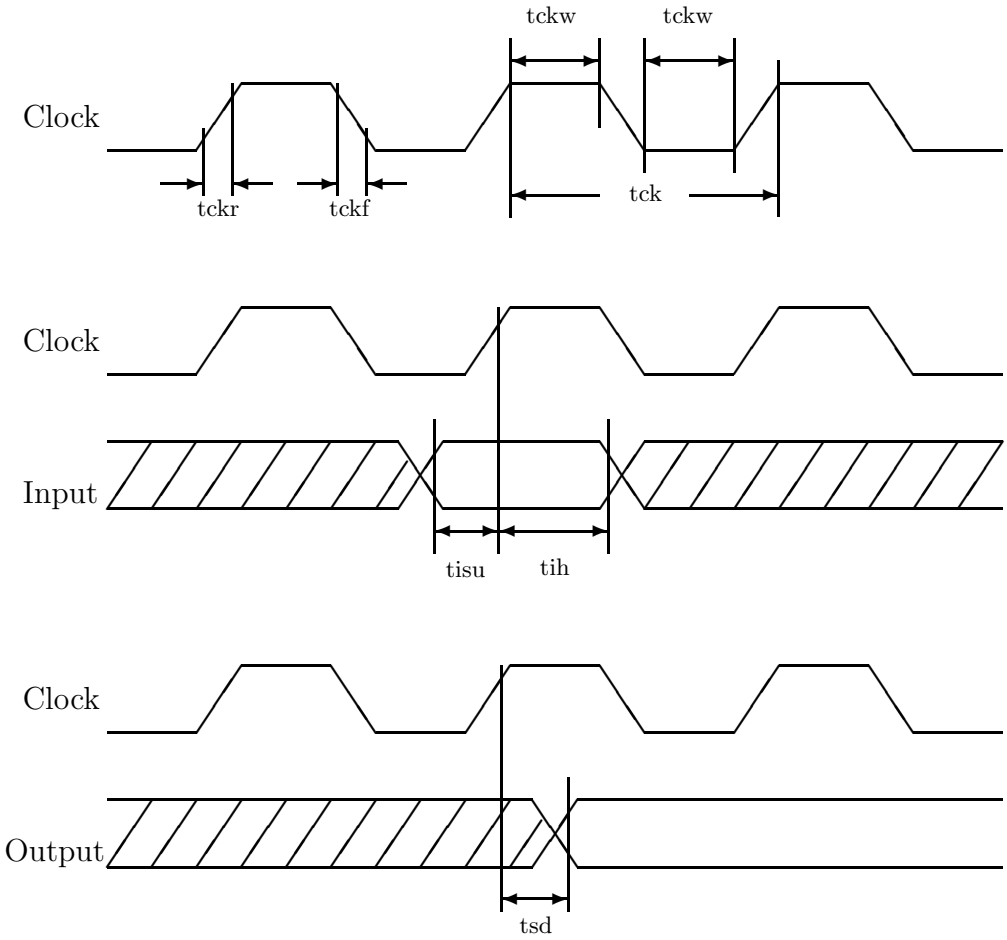

Figure 5: Timing for the encoder.