LDPC ENCODER SPECIFICATION VERSION 1.05

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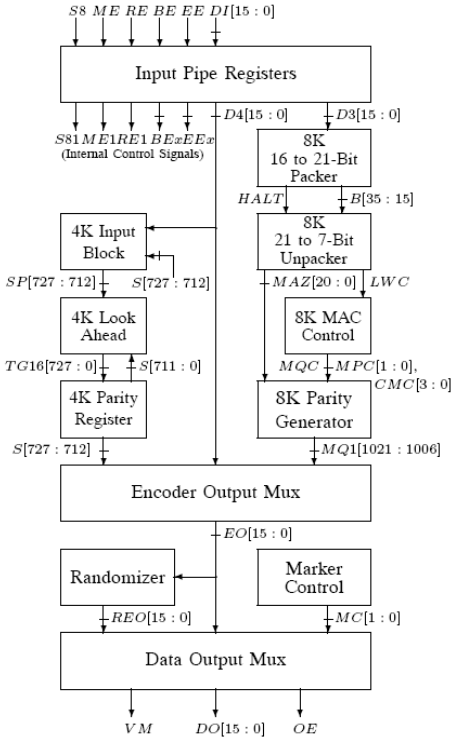
Features

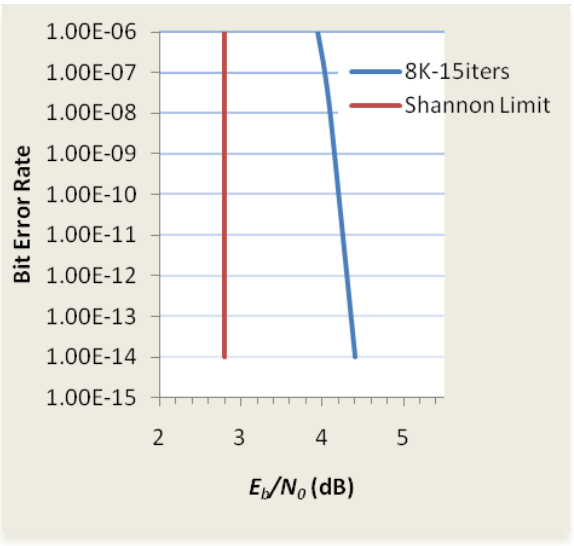
- Selectable (4088,3360) and (8158,7136) Low Density Parity Check Encoders
  - (4088,3360) code shortened from a (4095,3367) code
  - (8158,7136) code shortened from a (8176,7154) code[1]
- Selectable CCSDS standard randomizer[2]
- Selectable CCSDS standard frame marker[2]
- No error floor above 10^{-14} BER
- User programmable 32-bit frame marker
- 1 Gbit/s sustained data rate (with clock at 67 MHz)
- 16-bit parallel input and output width
- 3.3V Pad ring voltage
- 2.5V Core voltage
- TID > 100 KRad
- SEL Immune to 120 LET (Mev-cm^2/mg)
- Low SEU-induced error rate
- 68 pin ceramic QFP
- Typical power usage 1.3W at 67MHz
- Qualified to Level-1 space mission requirements

Applications

- Satellite RF communication links
- Optical communication
- Mass storage sub-system



LDPC Encoder Functional Block Diagram



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[1] *Low Density Parity Check Codes for Use in Near-Earth And Deep Space Applications*, Experimental Specifications, CCSDS 131.1-O-2, Orange Book, September 2007

[2] *TM Synchronization and Channel Coding.* Recommendation for Space Data System Standards, CCSDS 131.0-B-1. Blue Book. Issue 1. September 2003

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1.0 GENERAL DESCRIPTION

This chip implements two low density parity check (LDPC) codes.

1.1 LDPC 4K code

The (4088,3360) LDPC code is shortened from a geometry-based (4095,3367) cyclic code designed to have an error floor no higher than 10^{-10} BER. The code is specified by the following generator polynomial.

$$g(x) = x^0+x^2+x^4+x^6+x^8+x^{10}+x^{12}+x^{16}+x^{22}+x^{26}+x^{30}+x^{32}+x^{34}+x^{38}+x^{40}+x^{42}+x^{44}+x^{46}+x^{54}+x^{64}+x^{68}+x^{74}+x^{78}+x^{82}+x^{84}+x^{86}+x^{88}+x^{90}+$$
$$x^{92}+x^{94}+x^{98}+x^{106}+x^{110}+x^{112}+x^{114}+x^{118}+x^{122}+x^{124}+x^{128}+x^{134}+x^{138}+x^{150}+x^{152}+x^{156}+x^{160}+x^{162}+x^{166}+x^{168}+x^{170}+x^{172}+x^{176}+x^{180}+x^{182}$$
$$+x^{184}+x^{186}+x^{190}+x^{197}+x^{199}+x^{200}+x^{201}+x^{203}+x^{204}+x^{205}+x^{206}+x^{207}+x^{208}+x^{210}+x^{211}+x^{212}+x^{214}+x^{215}+x^{216}+x^{217}+x^{218}+x^{220}+x^{221}+x^{223}+$$
$$x^{225}+x^{227}+x^{229}+x^{232}+x^{237}+x^{238}+x^{240}+x^{242}+x^{246}+x^{247}+x^{248}+x^{249}+x^{250}+x^{253}+x^{254}+x^{255}+x^{260}+x^{261}+x^{263}+x^{264}+x^{265}+x^{266}+x^{269}+x^{270}+$$
$$x^{272}+x^{273}+x^{274}+x^{275}+x^{276}+x^{277}+x^{279}+x^{280}+x^{281}+x^{282}+x^{283}+x^{284}+x^{285}+x^{286}+x^{290}+x^{291}+x^{292}+x^{293}+x^{295}+x^{296}+x^{298}+x^{300}+x^{301}+x^{303}+$$
$$x^{307}+x^{310}+x^{312}+x^{314}+x^{319}+x^{321}+x^{322}+x^{323}+x^{325}+x^{328}+x^{330}+x^{331}+x^{334}+x^{335}+x^{336}+x^{340}+x^{342}+x^{344}+x^{345}+x^{346}+x^{349}+x^{350}+x^{353}+x^{355}+$$
$$x^{358}+x^{359}+x^{362}+x^{365}+x^{366}+x^{367}+x^{369}+x^{371}+x^{372}+x^{373}+x^{374}+x^{375}+x^{386}+x^{387}+x^{389}+x^{390}+x^{392}+x^{395}+x^{397}+x^{398}+x^{399}+x^{400}+x^{401}+x^{403}+$$
$$x^{406}+x^{408}+x^{409}+x^{411}+x^{412}+x^{415}+x^{416}+x^{417}+x^{418}+x^{419}+x^{420}+x^{421}+x^{422}+x^{423}+x^{425}+x^{433}+x^{434}+x^{439}+x^{441}+x^{442}+x^{446}+x^{447}+x^{452}+x^{453}+$$
$$x^{455}+x^{456}+x^{458}+x^{459}+x^{462}+x^{464}+x^{465}+x^{470}+x^{474}+x^{475}+x^{477}+x^{478}+x^{479}+x^{480}+x^{481}+x^{484}+x^{485}+x^{486}+x^{487}+x^{488}+x^{491}+x^{492}+x^{494}+x^{495}+$$
$$x^{496}+x^{498}+x^{499}+x^{501}+x^{505}+x^{507}+x^{510}+x^{511}+x^{513}+x^{514}+x^{521}+x^{524}+x^{525}+x^{526}+x^{529}+x^{533}+x^{536}+x^{537}+x^{542}+x^{545}+x^{546}+x^{548}+x^{549}+x^{553}+$$
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$$x^{598}+x^{558}+x^{600}+x^{601}+x^{604}+x^{607}+x^{608}+x^{611}+x^{612}+x^{614}+x^{615}+x^{618}+x^{620}+x^{624}+x^{626}+x^{634}+x^{638}+x^{642}+x^{646}+x^{650}+x^{658}+x^{662}+x^{666}+x^{672}+$$
$$x^{676}+x^{678}+x^{680}+x^{682}+x^{684}+x^{688}+x^{692}+x^{698}+x^{702}+x^{708}+x^{710}+x^{714}+x^{720}+x^{724}+x^{728}$$

This polynomial is the reciprocal polynomial of the (0,6)th-order Euclidean geometry code based on Euclidean geometry EG(2,2^6). Message data is input to the chip 16 bits at a time to allow a 16-bit look ahead scheme. By using look ahead, a 1 Gbit/s bit rate can be sustained using a 67 MHz system clock. The 210 16-bit data words are input to the chip and passed out of the chip with 6 clock cycles of latency when no frame marker is inserted. When the two-word frame marker is prepended, data has an 8 clock cycle latency. After the message words, forty six 16-bit parity words follow of which 45 are all parity bits. The final 16-bit output word contains the last 8 bits of parity with 0's appended.

1.2 LDPC 8K code

The (8158,7136) LDPC code is shortened from a geometry-based (8176,7154) quasi-cyclic code designed to have an error floor no higher than 10^{-10} BER. The code is specified by an 8176 x 1022 H matrix containing 32 right-circulant sub-matrices.

$$H=\left|\begin{matrix} C_{1,1} & C_{1,2} & C_{1,3} & C_{1,4} & C_{1,5} & C_{1,6} & C_{1,7} & C_{1,8} & C_{1,9} & C_{1,10} & C_{1,12} & C_{1,13} & C_{1,14} & C_{1,15} & C_{1,16} \\ C_{2,1} & C_{2,2} & C_{2,3} & C_{2,4} & C_{2,5} & C_{2,6} & C_{2,7} & C_{2,8} & C_{2,9} & C_{2,10} & C_{2,12} & C_{2,13} & C_{2,14} & C_{2,15} & C_{2,16} \end{matrix}\right|$$

Each $C_{i,j}$ is a 511 x 511 right-circulant matrix containing two ones per row and column. The column positions of the ones for the first row of the $C_{1,j}$ right-circulant matrices, are as follows:

0	176	523	750	1022	1374	1557	1964	2044	2436	2706	2964	3066	3417	3586	3936
4088	4395	4652	4928	5110	5317	5639	5902	6132	6531	6845	7100	7154	7401	7701	7926

The column positions of the ones, for the first row of the $C_{2,j}$ right-circulant matrices, are as follows:

99	471	641	984	1220	1457	1793	2011	2259	2464	2837	3036	3114	3462	3770	4022
4361	4518	4901	5050	5206	5489	5812	6007	6376	6599	7007	7113	7205	7536	7857	8079

Message data is input to the chip 16 bits at a time. A 1 Gbit/s bit rate can be sustained using a 67 MHz system clock. The 446 16-bit data words are input to the chip and passed out of the chip with 10 clock cycles of latency when no frame marker is inserted. When the two-word frame marker is prepended, data has a12 clock cycle latency. After the message words, sixty

four 16-bit parity words follow of which 63 are all parity bits. The final 16-bit output word contains the last 14 bits of parity with 0's appended.

2.0 CIRCUIT OPERATION

An overall block diagram is shown in Figure 1. Message data is input to the encoder block on the data input bus (DI). Data to be encoded is framed by the encode enable (EE) signal. The (8158,7136) code is selected by holding the select 8K (S8) input high. If S8 is low, the (4088,3360) code is selected. The message data and parity output by the encoder block will be randomized if randomize enable (RE) is asserted. An optional internal frame marker will precede the message data if the marker enable (ME) is asserted. Data will pass through the chip without being encoded by using a bypass mode if bypass enable (BE) is asserted. Message data output on the data output bus (DO) is framed by output enable (OE). Valid marker (VM) will flag, if correct, an external frame marker added during a bypass operation.

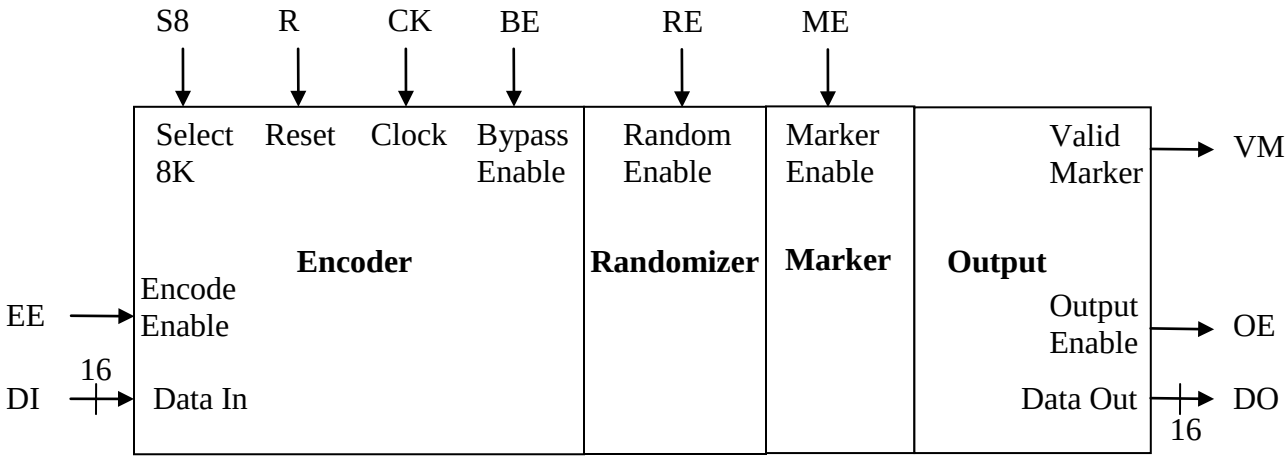


Figure 1: Block Diagram for the Encoder.

2.1 Initialization

Before proper circuit operation can begin, the encoder sections must be initialized by bringing the reset input (R) high for at least two clock pulses. Selection of the CCSDS standard frame marker is made by holding encode enable (EE) low while R is high. This loads the CCSDS frame marker value of 1ACF FC1D into the internal frame marker register. For a non-CCSDS frame marker, data on DI is shifted through the frame marker register during reset when EE is held high. Programming the frame marker register is accomplished by bringing EE low coincident with R transitioning low as shown in Figure 2. The final two words FM1 and FM2 on the data bus are then stored in the frame marker register. During reset, ME should be brought high to enable the frame marker or should be brought low to disable the frame marker. Since this chip contains two encoders, S8 must be held high to enable the (8158,7136) code or held low to enable the ((4088,3360) code. ME and S8 must remain in the selected states until another initialization occurs. EE should remain low after reset transitions low until data for encoding is presented on the data bus.

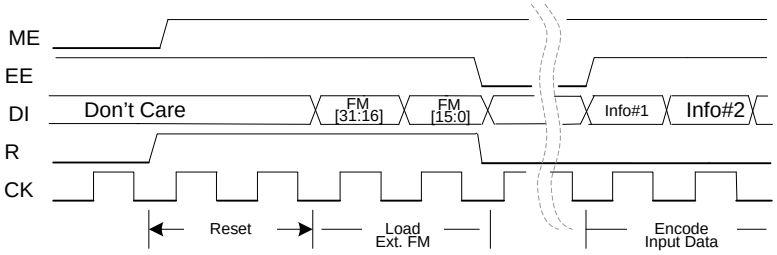


Figure 2: Timing Diagram for Programming a Non-CCSDS Frame Marker value.

Two clock pulses after R is brought low, circuit operation may commence. The circuit may be re-initialized at any time, but any messages being processed by the encoder section at that time will be lost.

2.2 Encoder Operation

Encoding is performed by operating on message bits presented to the encoder 16 bits at a time on the data input bus (DI). The first bit of the message is presented on the most significant bit of the data bus, DI[15], with the first data word. EE is brought high coincidentally with the first word of message data to be encoded. For the 8K code, EE must remain high until 446 words of message data have been clocked into the encoder on DI or for 210 words for the 4K code. For the 8K code,18 zeros are internally prepended to the shortened incoming data before the encoding process begins. For the 8K code, the input data appears on the output data bus (DO) ten clock cycles after being presented on DI if ME=0 or following the prepended frame marker at the twelfth clock cycle if ME=1. For the 4K code, the input data appears on the output data bus (DO) six clock cycles after being presented on DI if ME=0 or following the prepended frame marker at the eighth clock cycle if ME=1. Data is clocked in and out of the integrated circuit on the rising edge of the clock (CK).

EE is brought low again when the last message data has been clocked into the integrated circuit. For the 8K code, EE must remain low at least 64 clock cycles if ME=0 or 66 clock cycles if ME=1, during which time 64 16-bit words follow of which 63 are all parity bits. The last 14 bits of parity are DO[15:2] of the 64^{th} parity word. DO[1:0] of the last parity word are 0's. If ME=1, holding EE low for at least 66 clock cycles allows room for the frame marker to proceed the following block of data. For the 4K code, EE must remain low at least 46 clock cycles if ME=0 or 48 clock cycles if ME=1, during which time 46 16-bit words follow of which 45 are all parity bits. The last 8 bits of parity are DO[15:8] of the 46^{th} parity word. DO[7:0] of the last parity word are 0's. If ME=1, holding EE low for at least 48 clock cycles allows room for the frame marker to proceed the following block of data.

This operation also fills the parity generator with zeros. For the 8K code, if EE is held low longer than 64/66 clock cycles, zeros will appear on the data output bus. Bringing EE high after it has been low for 64/66 or more clock cycles starts the processing of the next set of message data. For the 4K code, if EE is held low longer than 46/48 clock cycles, zeros will appear on the data output bus. Bringing EE high after it has been low for 46/48 or more clock cycles starts the processing of the next set of message data. Figure 3 shows the timing for EE with ME=0.

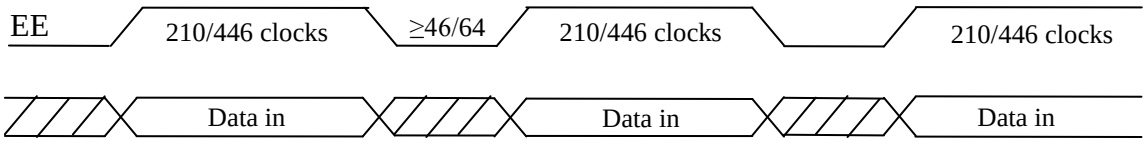


Figure 3: Timing Diagram for the EE signal.

2.3 Bit Packing

For the 8K code, Figure 4a represents the original codeword. The chip works on a shortened version of the LDPC code, as shown in Figure 4b. In order to recreate the full message prior to encoding, eighteen 0's are prepended to the message data. These eighteen 0's are not output on the data bus and are referred to as virtual fill. The first bit of input data is output on DO[15] during the first of 446 16-bit data words containing the message data (446x16=7130 message bits). Sixty four 16-bit words follow of which 63 are all parity bits. The final 16-bit output word contains the last 14 bits of parity (63x16+14=1022 parity bits) with two actual fill 0's appended (1022 parity bits + 2 fill bits = 64x16). The decoder would effectively prepend eighteen 0's to the received data prior to decoding. This shortened code allows easy interface to 16-bit and 32-bit system busses.

For the 4K code, Figure 5a represents the original codeword. The chip works on a shortened version of the LDPC code, as shown in Figure 5b. In order to recreate the full message prior to encoding, seven 0's are prepended to the message data. These seven 0's are not output on the data bus and are referred to as virtual fill. The first bit of input data is output on DO[15] during the first of 210 16-bit data words containing the message data (210x16=3360 message bits). Forty six 16-bit words follow of which 45 are all parity bits. The final 16-bit output word contains the last 8 bits of parity (46x16+8=728 parity bits) with eight actual fill 0's appended (728 parity bits + 8 fill bits = 46x16). The decoder would effectively prepend seven 0's to the received data prior to decoding. This shortened code allows easy interface to 16-bit and 32-bit busses.

a)

	1	2		447	448		510	511
DO[15]	m1	m17		m7137	m7153		p991	p1007
DO[14]	m2	m18		m7138	m7154		p992	p1008
DO[13]	m3	m19		m7139	p1		p993	p1009
DO[12]	m4	m20		m7140	p2		p994	p1010
DO[11]	m5	m21		m7141	p3		p995	p1011
DO[10]	m6	m22		m7142	p4		p996	p1012
DO[9]	m7	m23		m7143	p5		p997	p1013
DO[8]	m8	m24	…	m7144	p6	…	p998	p1014
DO[7]	m9	m25		m7145	p7		p999	p1015
DO[6]	m10	m26		m7146	p8		p1001	p1016
DO[5]	m11	m27		m7147	p9		p1002	p1017
DO[4]	m12	m28		m7148	p10		p1003	p1018
DO[3]	m13	m29		m7149	p11		p1004	p1019
DO[2]	m14	m30		m7150	p12		p1006	p1020
DO[1]	m15	m31		m7151	p13		p1005	p1021
DO[0]	m16	m32		m7152	p14		p1006	p1022

b)

	V	V	1	2		446	447		509	510
DO[15]		0	m1	m17		m7121	p1		p993	p1009
DO[14]		0	m2	m18		m7122	p2		p994	p1010
DO[13]		0	m3	m19		m7123	p3		p995	p1011
DO[12]		0	m4	m20		m7124	p4		p996	p1012
DO[11]		0	m5	m21		m7125	p5		p997	p1013
DO[10]		0	m6	m22		m7126	p6		p998	p1014
DO[9]		0	m7	m23		m7127	p7		p999	p1015
DO[8]		0	m8	m24	…	m7128	p8	…	p1000	p1016
DO[7]		0	m9	m25		m7129	p9		p1001	p1017
DO[6]		0	m10	m26		m7130	p10		p1002	p1018
DO[5]		0	m11	m27		m7131	p11		p1003	p1019
DO[4]		0	m12	m28		m7132	p12		p1004	p1020
DO[3]		0	m13	m29		m7133	p13		p1005	p1021
DO[2]		0	m14	m30		m7134	p14		p1006	p1022
DO[1]	0	0	m15	m31		m7135	p15		p1007	0
DO[0]	0	0	m16	m32		m7136	p16		p1008	0

Figure 4: a) Original 8K Bit Packing Diagram b) Shortened 8K Bit Packing Diagram.

a)

	1	2		210	211		255	256
DO[15]	m1	m17		m3345	m3361		p698	p714
DO[14]	m2	m18		m3346	m3362		p699	p715
DO[13]	m3	m19		m3347	m3363		p700	p716
DO[12]	m4	m20		m3348	m3364		p701	p717
DO[11]	m5	m21		m3349	m3365		p702	p718
DO[10]	m6	m22		m3350	m3366		p703	p719
DO[9]	m7	m23		m3351	m3367		p704	p720
DO[8]	m8	m24	…	m3352	p1	…	p705	p721
DO[7]	m9	m25		m3353	p2		p706	p722
DO[6]	m10	m26		m3354	p3		p707	p723
DO[5]	m11	m27		m3355	p4		p708	p724
DO[4]	m12	m28		m3356	p5		p709	p725
DO[3]	m13	m29		m3357	p6		p710	p726
DO[2]	m14	m30		m3358	p7		p711	p727
DO[1]	m15	m31		m3359	p8		p712	p728
DO[0]	m16	m32		m3360	p9		p713	

b)

	V	1	2		210	211		255	256
DO[15]		m1	m17		m3345	p1		p705	p721
DO[14]		m2	m18		m3346	p2		p706	p722
DO[13]		m3	m19		m3347	p3		p707	p723
DO[12]		m4	m20		m3348	p4		p708	p724
DO[11]		m5	m21		m3349	p5		p709	p725
DO[10]		m6	m22		m3350	p6		p710	p726
DO[9]		m7	m23		m3351	p7		p711	p727
DO[8]		m8	m24	…	m3352	p8	…	p712	p728
DO[7]		m9	m25		m3353	p9		p713	p729
DO[6]	0	m10	m26		m3354	p10		p714	p730
DO[5]	0	m11	m27		m3355	p11		p715	p731
DO[4]	0	m12	m28		m3356	p12		p716	p732
DO[3]	0	m13	m29		m3357	p13		p717	0
DO[2]	0	m14	m30		m3358	p14		p718	0
DO[1]	0	m15	m31		m3359	p15		p719	0
DO[0]	0	m16	m32		m3360	p16		p720	0

Figure 5: a) Original 4K Bit Packing Diagram b) Shortened 4K Bit Packing Diagram.

2.4 Bypass Operation

After a reset or after a block has been encoded and the parity read from the chip, and if ME=0, a data bypass operation can occur. Data can flow through the encoder without being encoded by bringing BE high coincidentally with the first word of data to be passed unprocessed through the chip. After the ten clock cycles of latency for an 8K code or the six clock cycles of latency for the 4K code, the data entering on DI appears on DO and continues to pass through the chip as long as BE remains high. While BE is high, EE must be held low to hold the registers in the parity generator reset. A bypass operation can be used to insert an externally generated frame marker.

2.5 Randomizer

A pseudo-random sequence generated by $h(x)=x^8+x^7+x^5+x^3+1$ is applied to the data and parity if RE=1. The 255-bit sequence is bitwise exclusive ORed with the code word. The sequence generator is initialized to the all ones state at the beginning of each code word. The frame marker is not affected by the randomizer regardless of the state of RE. Zero's appearing on the output bus between code words will be randomized if RE=1. The sequencer begins operation on the first bit of message data in the codeword. If RE=1 in bypass mode, the bypass data will be processed through the randomizer. An unrandomized frame marker can be included in the randomized bypass data by bringing RE low coincident with the first word of unrandomized frame marker and bringing it high after the last word of frame marker as shown in Figure 6.

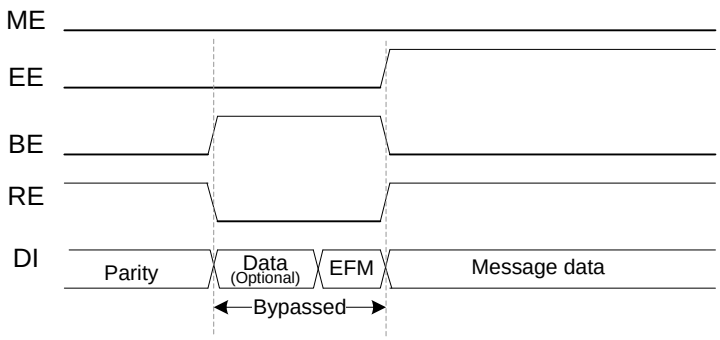


Figure 6: Timing Diagram for an External Frame Marker (EFM).

2.6 Frame Marker

An internally generated 32-bit frame marker is output in two 16-bit words if ME=1. This frame marker can be either the attached synchronization marker for non-turbo-coded data specified in the CCSDS standard as the following hex sequence: 1ACF FC1D or a user programmed 32-bit sequence entered during initialization. This frame marker is output in the two clock cycles preceding the first word of message data in a code block.

2.7 VM Output

An externally generated frame marker can be introduced with a bypass operation. For the default CCSDS sequence, whenever a bypass operation immediately precedes an encoding operation, if the last two 16-bit words of bypassed data are 1ACF followed by FC1D then the Valid Marker (VM) output will be a 1 as these two words are output on DO as shown in Figure 7.

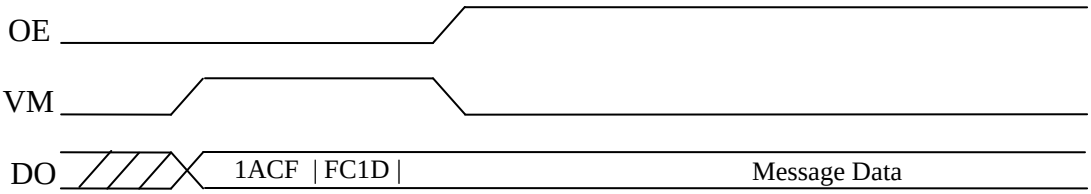


Figure 7: Timing Diagram for Valid Marker.

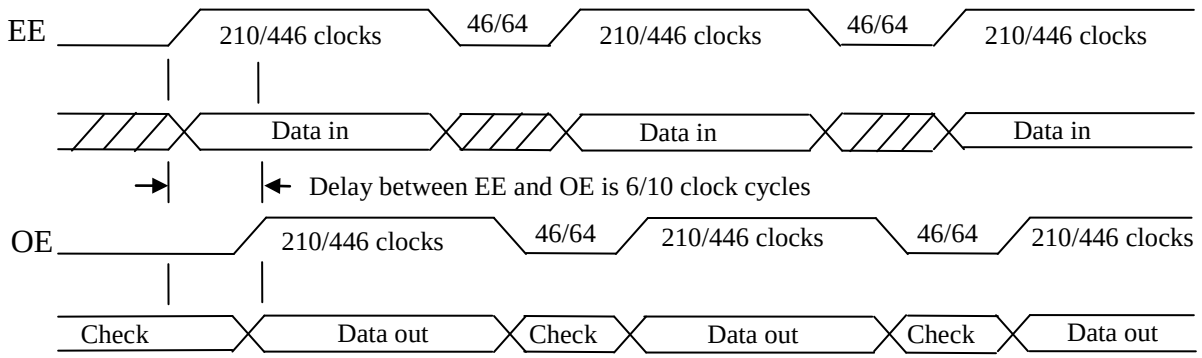


Figure 8: Overall Timing Diagram for the Encoder with ME=0.

2.8 DO and OE Outputs

The latency of data through the encoder is ten clock cycles if ME=0 and twelve clock cycles if ME=1 for the 8K code. The latency of data through the encoder is six clock cycles if ME=0 and eight clock cycles if ME=1 for the 4K code. Thus, ten/twelve clock cycles for the 8K code or six/eight clock cycles for the 8K code after EE is brought high, the output enable (OE) goes high specifying the start of message data in a valid code word. When OE goes low, the encoder is outputting the parity bits. Thus OE frames the message data and is only high when message data is being output. An overall timing diagram for the encoder is shown in Figure 8 for ME=0. When ME=1, Figure 9 applies.

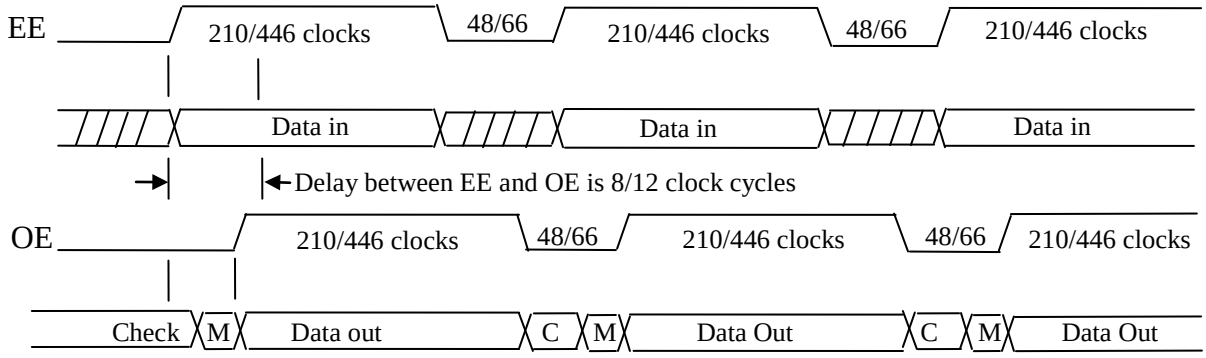


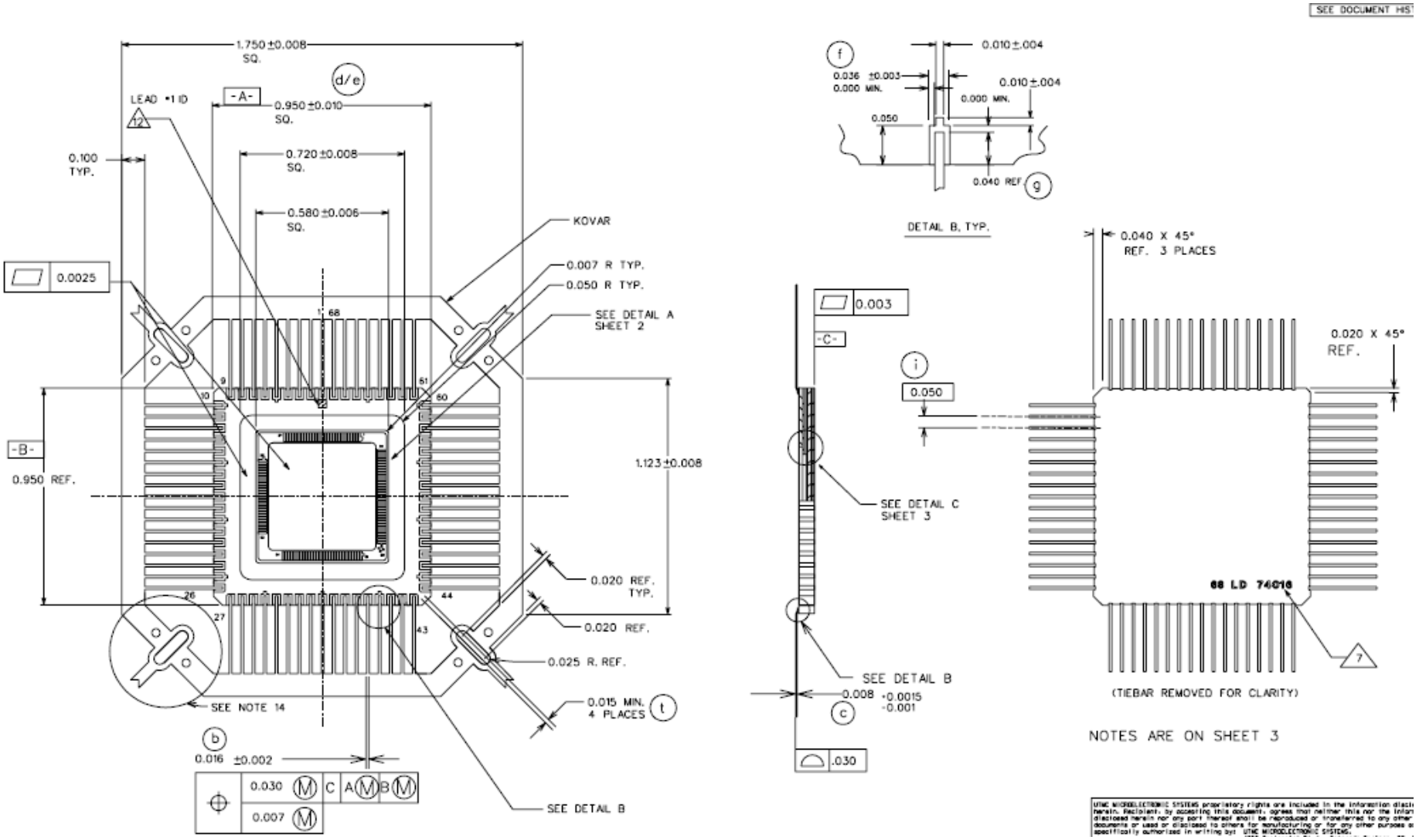
Figure 9: Overall Timing Diagram for the Encoder with ME=1.

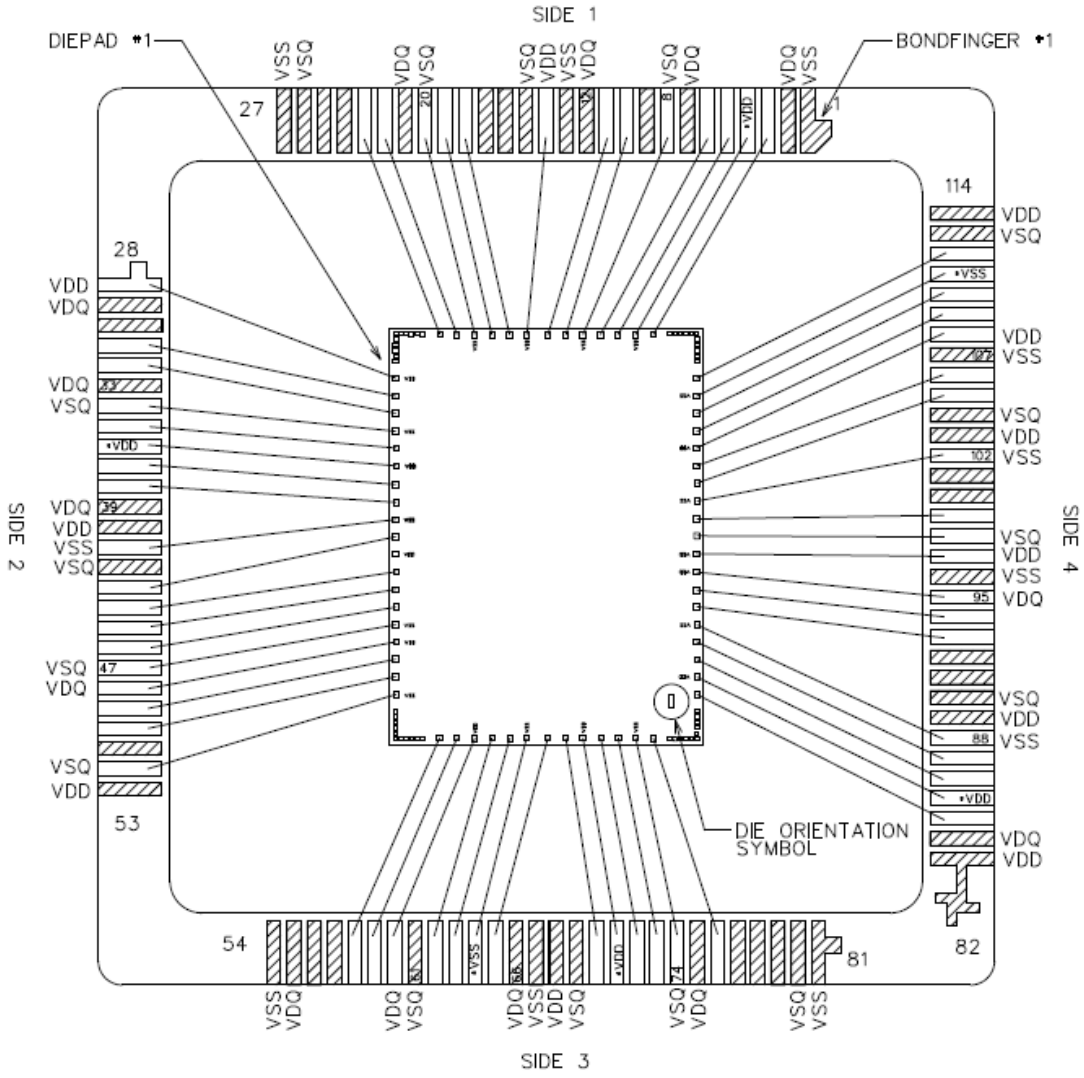
3.0 PIN DESCRIPTION

3.1 Top Level Diagram and Pin List

Table 3.1: Pin list		
Name	Type	Description
CK	input	Clock is the master clock for the chip. Data and control are clocked in on the rising edge.
R	input	Reset, active HIGH. R initializes the registers in the parity generator as well as all the control flip flops. The signal must be held high at least two clock cycles.
EE	input	Enable encode, active HIGH. EE frames the input message words. The signal is brought high coincidentally with the first word of data and is brought low after the last word of data.
BE	input	Bypass enable, active HIGH. BE frames input words that should pass through the encoder without being encoded. The signal is brought high coincidentally with the first word of data and is brought low after the last data word.
RE	input	Randomize enable, active HIGH. RE is normally set high during initialization and remains high until the next Initialization if the data, parity, and inter-block zeros should be randomized. RE can be pulsed low during a bypass operation coincident with an external frame marker.
ME	input	Marker enable, active HIGH. ME is set high during initialization and remains high until the next initialization if a Frame marker is to be inserted before each codeword.
S8	input	Select 8K, active HIGH. S8 is set high during initialization and remains high until the next initialization to enable the (8158,7136) code. If set low during initialization and held low the (4088,3360) code is enabled.
OE	output	Output Enable, active HIGH. OE frames the output message words. The signal goes high coincidentally with the first word of output data and goes low after the last output data word. This signal is EE delayed by the chip latency of 10/12 clock cycles for the 8K code or 6/8 clock cycles for the 4K code.
VM	output	Valid Marker, active HIGH. VM flags an external marker as valid if the 32-bit sequence is 1ACF FC1D. The signal goes high coincidentally with the first word of a correct output frame marker (1ACF) and goes low after the last word (FC1D).
DI[15:0]	input	Data Inputs. Bit 15 is the first bit in.
DO[15:0]	output	Data Outputs. Bit 15 is the first bit out.

4.0 PINOUT AND PACKAGE DESCRIPTION





CONNECTION TABLE												
SIDE 1			SIDE 2			SIDE 3			SIDE 4			
	B/F	PIN		B/F	PIN		B/F	PIN		B/F	PIN	
	1	VSS		28	VDD		54	VSS		82	VDD	
	2	VDQ		29	VDQ		55	VDQ		83	VDQ	
	3	61		30	10		56	27		84	44	
	4	62		31	11		57	28		85	45	
	5	63		32	15		58	29		86	46	
	6	64		33	VDQ		59	30		87	47	
	7	VDQ		34	VSQ		60	VDQ		88	VSS	
	8	VSQ		35	16		61	VSQ		89	VDD	
	9	65		36	17		62	31		90	VSQ	
	10	66		37	18		63	32		91	48	
	11	67		38	19		64	33		92	49	
	12	VDQ		39	VDQ		65	34		93	50	
	13	VSS		40	VDD		66	VDQ		94	51	
	14	VDD		41	VSS		67	VSS		95	VDQ	
	15	VSQ		42	VSQ		68	VDD		96	VSS	
	16	2		43	20		69	VSQ		97	VDD	
	17	3		44	21		70	35		98	VSQ	
	18	4		45	22		71	37		99	52	
	19	5		46	23		72	38		100	53	
	20	VSQ		47	VSQ		73	39		101	54	
	21	VDQ		48	VDQ		74	VSQ		102	VSS	
	22	6		49	24		75	VDQ		103	VDD	
	23	7		50	25		76	40		104	VSQ	
	24	8		51	26		77	41		105	55	
	25	9		52	VSQ		78	42		106	56	
	26	VSQ		53	VDD		79	43		107	VSS	
	27	VSS					80	VSQ		108	VDD	
							81	VSS		109	57	
										110	58	
										111	59	
										112	60	
										113	VSQ	
										114	VDD	

0.002

PWR & GND EXTERNAL PIN ASSIGNMENT TABLE				
SIDE	VDD	VSS	VDDQ	VSSQ
1	1	68	----	-----
2	-----	-----	13	12, 14
3	-----	36	-----	-----
4	-----	-----	-----	-----

Pinout:

Pin number	Signal name	Pin number	Signal name
1	DVDD	35	DI[8]
2	NC	36	DVSS
3	DO[12]	37	VDD
4	DO[13]	38	DI[7]
5	DVSS	39	DI[6]
6	DO[14]	40	DI[5]
7	DO[15]	41	NC
8	NC	42	NC
9	NC	43	NC
10	OE	44	DI[4]
11	VM	45	VDD
12	VSS	46	DI[3]
13	VDD	47	DI[2]
14	VSS	48	NC
15	DVSS	49	NC
16	S8	50	DI[1]
17	VDD	51	DI[0]
18	ME	52	DO[0]
19	RE	53	DO[1]
20	CK	54	NC
21	BE	55	DO[2]
22	EE	56	DO[3]
23	R	57	DO[4]
24	DI[15]	58	DO[5]
25	DI[14]	59	DVSS
26	NC	60	DO[6]
27	NC	61	DO[7]
28	NC	62	DVDD
29	DI[13]	63	DO[8]
30	DI[12]	64	DO[9]
31	DI[11]	65	DVSS
32	DI[10]	66	DO[10]
33	VSS	67	DO[11]
34	DI[9]	68	DVSS

5.0 ELECTRICAL SPECIFICATION

Note that care must be taken on output pads to limit ringing to be no greater than 4.2V and no less than -0.8V.

5.1 Absolute Maximums

SYMBOL	PARAMETER	LIMITS
VDD	Power Supply	-0.3 to 2.95 Volts
DVDD	IO Power Supply	-0.3 to 3.8 Volts
$V_{I/O}$	Voltage on any given pin	-0.3 to 3.8 Volts
T_{STOR}	Storage temperature	-65 to 150 C

5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	LIMITS
VDD	Power Supply	2.4 to 2.8 Volts
DVDD	IO Power Supply	3.0 to 3.6 Volts
$V_{I/O}$	Voltage on any given pin	-0.3 to 2.75 Volts
$T_{JUNCTION}$	Junction operating temperature	-55 to 125 C
T_{JC}	Thermal junction to case resistance	5 C/W

5.3 Operating Characteristics

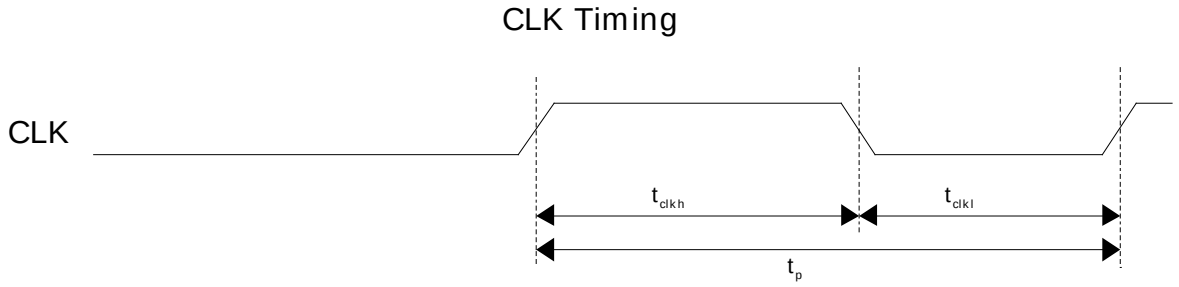
SYMBOL	PARAMETER	Min.	Typ	Max.	Units	Conditions
VIH(min)	Min. High Level Input Voltage	0.7 * V_{DVDD}			volts	Guaranteed Logic '1'
VIL(max)	Max. Low Level Input Voltage			0.3 * V_{DVDD}	volts	Guaranteed Logic '0'
VIHC(min)	Min. High Level Input Voltage, High CLOCK Input	0.9 * V_{DVDD}			volts	Guaranteed Logic '1'
VILC(max)	Max. Low Level Input Voltage, Low CLOCK Input			0.1 * V_{DVDD}	volts	Guaranteed Logic '0'
VOH(min)	Min. High Level Output Voltage High	0.9 * V_{DVDD}			volts	
VOL(max)	Max. Low Level Output Voltage Low			0.1 * V_{DVDD}	volts	
IIH	High Level Input Current			1	µA	Vin = VDD (pure input)
IIL	Low Level Input Current			-1	µA	Vin =VSS (pure input)
$IMAX_{DVDD}$	Maximum I/O operating current			0.15	A	@67 MHz and max voltage and max utilization, max output loading
$IMAX_{VDD}$	Maximum core operating current			0.25	A	@67 MHz and max voltage and max utilization
QI_{VDD}	Maximum Quiescent VDD current at 25C and 50Krad total dose[2]			150 uA		
QI_{DVDD}	Maximum Quiescent DVDD current at 25C and 50Krad total dose[2]			300 uA		

[2]Assuming dose rates below 40 millirads/second.

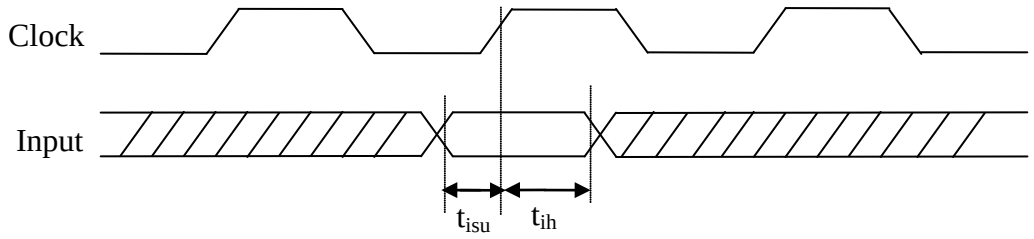
5.4 Power-Up Sequence

VDD must be brought up before or in conjunction with DVDD. DVDD must not be high while VDD is low as it results in a high current state in the level shifters within the pads.

5.5 Timing Diagrams



SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{clke}	CLK rise/fall time.		0.5	ns
t_p	Clock period. Must be greater than or equal to 15 ns.	15		ns
t_{clkh}	Clock high time.	55%	45%	cycle
t_{clkl}	Clock low time.	45%	55%	cycle



SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{isu}	Input setup to rising edge of clock.	2		ns
t_{ih}	Input hold past rising edge of clock.	0		ns
t_{sd}	Output delay past rising edge of clock.		6.5	ns