Radiation Tolerance at Modern Deep Sub-Micron Process Nodes and ICs' SRL Technology

Gary Maki, Sterling Whitaker, Eric Cameron, Lowell Miles, and Joe Feeley
ICS, LLC, PO Box 2236, 2040 Warren Wagon Road, McCall, ID 83638
gary.maki@ics-rhbd.com
sterling.whitaker@ics-rhbd.com

Introduction

Radiation tolerant microelectronic design and implementation is a complex subject with many considerations and nuances. Modern fabrication processes and techniques afford great opportunities for applications to the space environment, but also pose significant implementation challenges.

ICs has robust radiation tolerant technology, and the expertise to leverage it in modern deep sub-micron traditional bulk CMOS and SOI processes to provide error free operation. By contrast, other available solutions rely on complicated failure analysis of error prone legacy radiation tolerant technology.

Radiation Tolerance in Modern Processes

In some ways, modern microelectronic processes are inherently more radiation tolerant than prior process nodes, but they are also less robust in other ways, as illustrated in Figure 1. Increased tolerance to long term Total Ionizing Dose (TID) effects is mainly due to the reduction in gate oxide volume and Single Event Latch-up (SEL) improvement is driven primarily by the decrease in power supply voltage. Further mitigation can be accomplished through radiation tolerance by design (RHBD) methodologies.

Due in part to these same process changes, modern microelectronics are, however, increasingly susceptible to Single Event Upset (SEU). SEU tolerance is provided largely through application of RHBD methodologies. (Amort, et al., 2011). In addition to what is shown in Figure 1, as the speed of the electronics increases, SEU protection provided by legacy RHBD methodologies drops precipitously (Miles, Cameron, Whitaker, Maki, & Feeley, 2015), as shown in Figure 3.

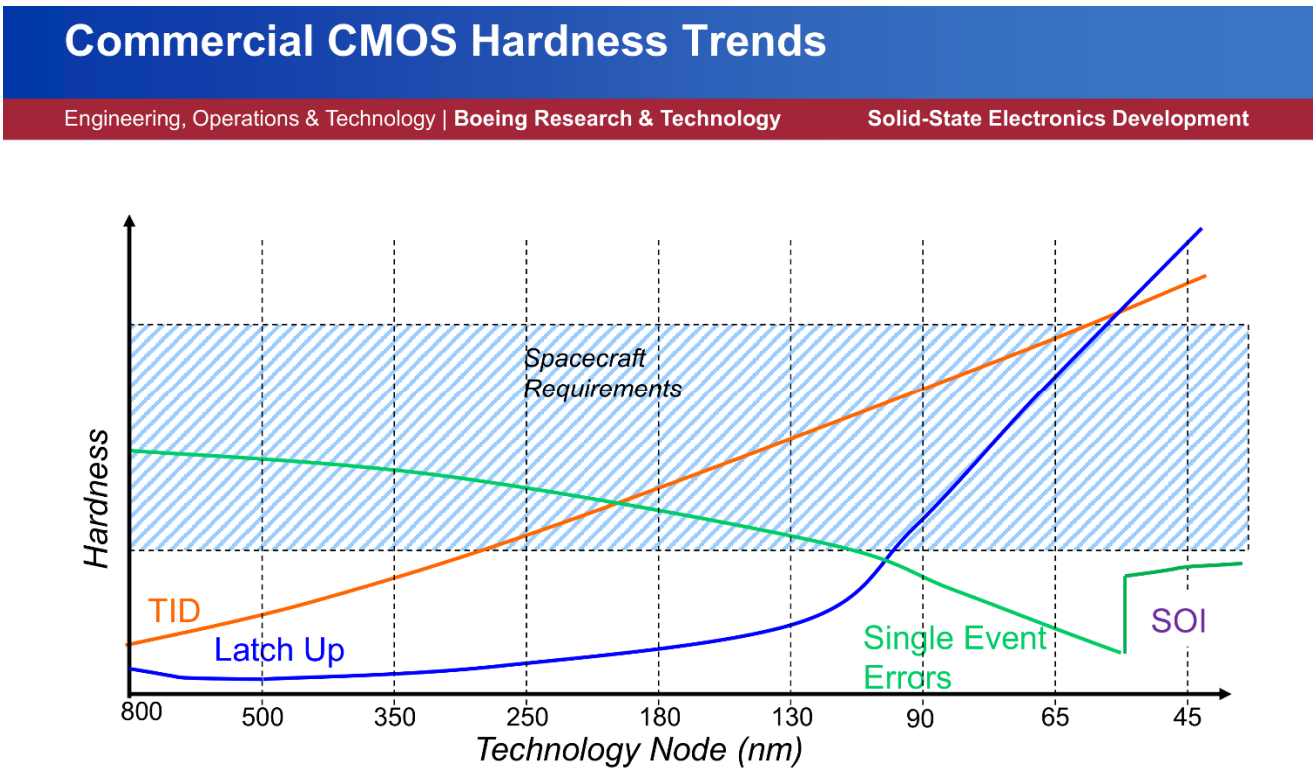

Figure 1: Radiation effects tolerance gained through legacy RHBD methodologies and Process Node evolution: Commercial process improvements reduce the need for TID and SEL Mitigation. Legacy RHBD techniques have been proving less effective at mitigating SEU as process geometries decrease (Amort, et al., 2011).

Certain fabrication processes, such as Silicon on Insulator (SOI), can help mitigate SEU as well, but come at a substantial cost penalty, and still require RHBD methodologies.

RHBD is accomplished using additional circuitry to either restore upset node values or to correct the consequences of upset nodes. The major addition is use of a radiation tolerant (RT) flip flop (FF) in critical areas of the design. Non-RT FFs are fundamentally 1-bit memory elements based on 2 state variable asynchronous sequential latch circuits. Legacy RT latches such as DICE and SERT are based on 4 state variable latches. Modern process nodes enable clock rates well in excess of 100MHz, which is beyond the capabilities of legacy RT FFs. Self-Restoring Logic (SRL) FFs use 6 state variable latches to protect against SEU at these rates.

Additional RHBD design methodologies include architectural level additions such as error correction based on added parity bits or triplication and voting. (Miles, Cameron, Whitaker, Maki, & Feeley, 2015).

Given that legacy NASA and DoD SEU tolerant cell designs have been shown not to provide protection for high speed circuits, Triple Modular Redundancy (TMR) is the only other legacy option. TMR, however, has several drawbacks. TMR requires triplication of flip-flops and data logic along with triplicated voters. Several existing instantiations of TMR require at least 80% more transistors than ICs' SRL technology. In addition, masked faults can exist with voter logic making testing difficult. SRL possesses the ability to allow complete testing to verify internal functionality.

Other groups have recommended the continued use of legacy RHBD technology, such as DICE, but following up with sophisticated failure simulation and analysis to determine error rates and mitigation

strategies. Utilizing truly SEU tolerant RHBD technology is a more straightforward and robust solution.

Self-Restoring Logic (SRL)

ICs' new RHBD technology, SRL, provides highly effective RHBD SEU mitigation. This technology is especially effective for high speed circuits implemented in small process geometries in either traditional bulk CMOS or SOI processes. SRL protects against SEU, regardless of the circuit speed, Figure 2. In contrast, legacy RHBD cells recover from SEU, but recovery takes time, and protection fails when SEU duration is significant compared with clock speed. (Miles, Cameron, Whitaker, Maki, & Feeley, 2015). Though this document's focus is specifically on radiation tolerance, ICs' technology is fault tolerant in general, and can provide protection from a wide variety of both hard and soft faults.

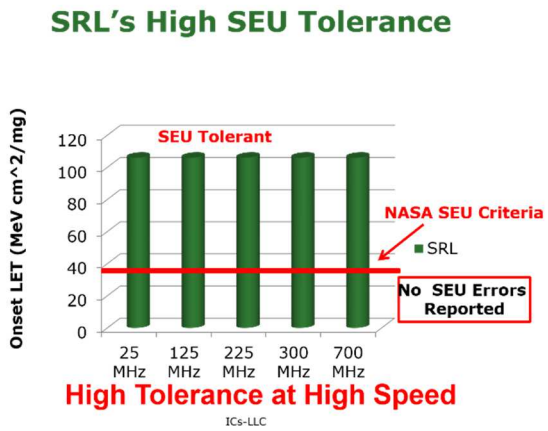

Figure 2: SRL flip flop SEU tolerance is not degraded by high clock rate operation.

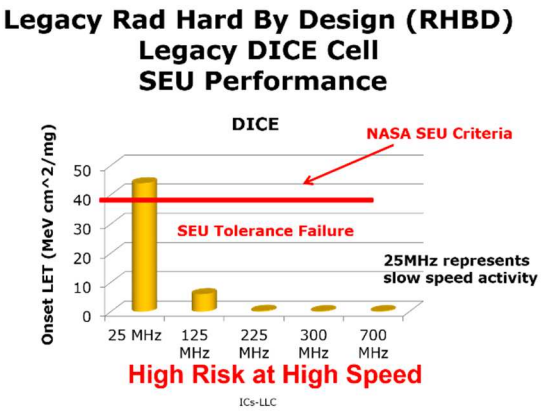

Figure 3: DICE flip flops fail to protect against SEU as clock rate increases.

Individual fabrication process nodes vary in their tolerance to radiation induced effects, and should be subjected to radiation testing to determine RHBD level and details required. Though SRL should work well in deep sub-micron SOI processes, it is also expected to be very effective implemented in a given deep sub-micron traditional bulk process. Due to a solid mathematical foundation, SRL will continue to provide robust SEU protection as process node geometries shrink and circuit speeds increase.

Additional observations can be used to lessen the area, power, and speed impact of implementing an SEU tolerant design. Depending on the requirements, it is possible that only critical portions of a design need to be protected. Data errors can be corrected with an Error Correcting Code (ECC), an Arithmetic Code (AC), or can often just be ignored, if such an error merely results in, for example, a few erroneous pixels on a flat screen. However an error in the control, especially the real time control electronics, is far more serious, and such control should be SEU tolerant. In such a scenario, one could design a fault tolerant controller and use ECC or AC for the data path. The control logic is often a small percentage of the total chip hardware, making this approach effective and economical.

Who We Are

ICs would welcome the opportunity to discuss the radiation and general fault tolerance advantage of using SRL, particularly for high speed circuits, and work to characterize, explore and implement robust fault tolerant solutions.

The technology leaders at ICs have been developing radiation hard electronics for over 3 decades, and have pioneered several RHBD methodologies. They have demonstrated and applied their expertise in numerous ASICs currently operating in many NASA and DoD missions. For example, ICs' chips have flown in, or are being integrated into, numerous missions such as MMS, NEAR, CONTOUR, JPSS, Cobra Brass, TIMED, LDCM, Mars Odyssey, Suomi NPP, Ladsat-7, SDO, TRMM, EO-1, New Horizon, RXTE, WISE, GOES-R, TERRA, HST, SBIRS High, Chandra X-ray, IRIS, and AURA.

ICs has supplied custom radiation-tolerant ASICs to NASA and government contractors for the space program for over 15 years, and has a superb track record in providing solutions that meet and exceed mission specifications.

References

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