REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 09. Modify Table I footnote 3/ and add footnote 10/. Updated boilerplate. - tmh	98-10-26	Monica L. Poelking
B	Add device types 10 – 24. Modify Table I, editorial changes throughout. – tmh	98-12-14	Monica L. Poelking
C	Add die requirement and appendix A. Update boileplate. – phn	01-06-14	Thomas M. Hess

REV																				
SHEET																				
REV	B	B	B	B	B	C	B	B	C	C	C	C	C	C	C	C	C	C		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		

REV STATUS	REV	C	C	B	C	C	C	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

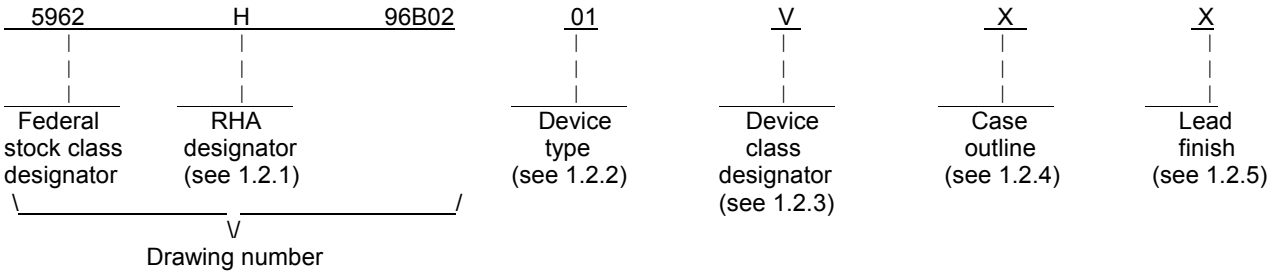
PMIC N/A	PREPARED BY Thomas M. Hess	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess	
	APPROVED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, CMOS, CUSTOM ASIC, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 96-09-16	
	REVISION LEVEL C	SIZE A CAGE CODE **67268** **5962-96B02** SHEET 1 OF 32

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN) in the applicable Altered Item Drawing (AID). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

Customizations (personalization) for each design, including circuit organization, electrical performance characteristics, and test conditions, shall be specified in an Altered Item Drawing (AID) (see 3.3 herein).

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Circuit (total number of usable gates)	Array family
01	<5,000 usable gates	UT25E/R
02	10,000 usable gates	UT25E/R
03	15,000 usable gates	UT25E/R
04	20,000 usable gates	UT25E/R
05	25,000 usable gates	UT25E/R
06	35,000 usable gates	UT35E/R
07	75,000 usable gates	UT75E/R
08	125,000 usable gates	UT100E/R
09	10,000 usable gates	UT25
10	15,000 usable gates	UT25
11	20,000 usable gates	UT25
12	25,000 usable gates	UT25
13	35,000 usable gates	UT35
14	75,000 usable gates	UT75
15	150,000 usable gates	UT150
16	200,000 usable gates	UT200
17	250,000 usable gates	UT250
18	300,000 usable gates	UT300
19	350,000 usable gates	UT350
20	400,000 usable gates	UT400
21	450,000 usable gates	UT450
22	500,000 usable gates	UT500
23	550,000 usable gates	UT550
24	600,000 usable gates	UT600

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style	θ_{JC} Thermal resistance
X	CQCC2-J84	84	Flatpack	1/
Y	CQCC1-F84	84	Flatpack	1/
Z	CQCC1-F132	132	Flatpack	1/
U	CQCC1-F172	172	Flatpack	1/
T	CQCC2-F172	172	Flatpack	1/
M	CQCC2-F196	196	Flatpack	1/
W	CMGA10-P281	281	Pin grid array	1/
N	(See figure 1)	224	Flatpack	2/
4	(See figure 1)	256	Flatpack	2/
5	(See figure 1)	304	Flatpack	2/
6	CMGA3-P85	85	Pin grid array	1/
7	CMGA17-P121	121	Pin grid array	1/
8	CMGA7-P145	145	Pin grid array	1/
9	CMGA21-P209	209	Pin grid array	1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 3/

Supply voltage range (V_{DD}) ..... -0.3 V dc to +7.0 V dc
Voltage at any pin range ($V_{I/O}$) ..... -0.3 V dc to V_{DD} + 0.3 V dc
Power dissipation (P_D) ..... as specified in the AID.
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 5 seconds) (T_{LS}) ..... +300EC
Latch-up immunity (I_{LU}) ..... ±150 mA
DC input current (I_I) ..... ±10 mA
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}) ..... +4.5 V dc to +5.5 V dc
Operating temperature range (T_C) ..... -55°C to +125°C
DC input voltage range (V_{IN}) ..... 0 V dc to V_{DD}

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) ..... As specified in the AID

1/ See MIL-STD-1835.
2/ As specified in the AID.
3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

1.6 Radiation features

Total dose (01-08)	1.0×10^6 rads(Si) 4/
Total dose (09)	1.0×10^5 rads(Si) 4/
Total dose (10 – 24)	1.0×10^5 rads(Si) 4/
Dose rate upset	
01 – 06	5.0×10^9 rads(Si)/sec 5/
07, 08, 09	1.0×10^9 rads(si)/sec 5/
10 – 24	1.0×10^9 rads(si)/sec 5/
Dose rate survivability	
01 – 06	1.0×10^{13} rads(Si)/sec 6/
07, 08	1.0×10^{12} rads(si)/sec 6/
09 – 24	$>1.0 \times 10^{11}$ rads(si)/sec 6/
SIngle event upset	$< 1.0 \times 10^{-10}$ errors per cell-day 6/ 7/
Linear energy threshold	$\leq$ 36 MeV/(mg/cm^2)
LET no upsets (see 4.4.4.4)	
Neutron fluence	1.0×10^{14} n/sq cm
Latchup	Latchup immune over maximum operating conditions

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

4/ Total dose Co-60 testing in accordance with MIL-STD-883, method 1019.
5/ Short pulse 20 ns FWHM (full width, half maximum).
6/ May be design dependent.
7/ SEU-hard flip-flop cell. Non-hard flip-flop cell is $5x\ 10^{-8}$ errors per cell-day.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M, shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Radiation exposure circuit. The radiation exposure circuit shall be as specified in figure 2.

3.3 AID requirements. All AIDs written against this SMD shall be sent to DSCC-VA. The following items shall be provided to the device manufacturer by the customer as part of an AID. Items 3.3.3 through 3.3.9 form a part of the manufacturer's design database/database archive. These items shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. As such, these items will not appear in the AID in the traditional sense.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.3 Functional block diagram (or equivalent VHDL behavioral description). 8/

3.3.4 Logic diagram (or equivalent structural VHDL description). 8/

3.3.5 Pin function description.

3.3.6 Design tape # or design document name (i.e., net list).

3.3.7 Design functional tape # or name.

3.3.8 Test functional tape # or name.

3.3.9 Switching waveform(s).

3.3.10 Fault coverage. The extent of fault coverage is controlled by the quality of the customers design input, therefore fault coverage shall be specified by the customer.

3.3.11 Device electrical performance characteristics. Device electrical performance characteristics shall include dc parametric (see table I herein for minimum requirements), functional, input to output ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended ambient operating temperature range and specified test load conditions.

3.3.12 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.13 Radiation hardness assurance. Additional radiation hardness requirements shall be specified in the AID.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

8/ If VHDL is utilized for documentation, a VHDL test bench shall be included for both behavioral and structural VHDL descriptions. Behavioral VHDL descriptions shall include function and timing at the port accurate enough to perform test generation and determine fault detection/fault isolation levels at the integrated circuits pins when performing board or subsystem simulations. For guidelines see DI-EGDS-80811.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID number shall be added to the marking by the manufacturer.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage low 3/	V_{OL1}	V_{DD} = 4.5 V, I_{OL} = 2.0 mA	1,2,3	All		0.4	V
	V_{OL2}	I_{OL} = 4.0 mA	1,2,3	All		0.4	
	V_{OL3}	I_{OL} = 8.0 mA	1,2,3	All		0.4	
	V_{OL4}	I_{OL} = 12.0 mA	1,2,3	All		0.4	
	V_{OL5}	I_{OL} = 1.0 µA	1,2,3	All		0.05	
	V_{OL6}	I_{OL} = 100 µA	1,2,3	All		0.25	
	V_{OL7}	I_{OL} = 100 µA	1,2,3	All		1.0	
Output voltage high 3/	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -2.0 mA	1,2,3	All	2.4		
	V_{OH2}	I_{OH} = -4.0 mA	1,2,3	All	2.4		
	V_{OH3}	I_{OH} = -8.0 mA	1,2,3	All	2.4		
	V_{OH4}	I_{OH} = -12.0 mA	1,2,3	All	2.4		
	V_{OH5}	I_{OH} = -1.0 µA	1,2,3	All	V_{DD}-0.05 V		
	V_{OH6}	I_{OH} = -100 µA	1,2,3	All	V_{DD}-0.25 V		
	V_{OH7}	I_{OH} = -100 µA	1,2,3	All	3.5		
Input leakage current 4/	I_{IN1}	V_{IN} = V_{DD} or V_{SS}	1,2,3	All	-1	+1	µA
	I_{IN2}	V_{IN} = V_{DD}	1,2,3	01-08	+150	+900	
	I_{IN2}	V_{IN} = V_{DD}	1,2,3	09 - 24	+150	+1300	
	I_{IN3}	V_{IN} = V_{SS}	1,2,3	All	-10	+10	
	I_{IN4}	V_{IN} = V_{SS}	1,2,3	All	-900	-150	
	I_{IN5}	V_{IN} = V_{DD}	1,2,3	All	-10	+10	
Output leakage current 5/	I_{OZ1}	V_O = V_{DD} and V_{SS}	1,2,3	All	-5	+5	
	I_{OZ2}		1,2,3	All	-10	+10	
	I_{OZ3}		1,2,3	All	-20	+20	
	I_{OZ4}		1,2,3	All	-30	+30	
Output current short-circuit 5/ 6/	I_{OS1}	V_O = V_{DD} and V_{SS}	1,2,3	All	-50	+50	mA
	I_{OS2}		1,2,3	All	-100	+100	
	I_{OS3}		1,2,3	All	-200	+200	
	I_{OS4}		1,2,3	All	-300	+300	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Quiescent supply current	I_{DDQ}	V_{DD} = 5.5 V	1,2,3	All		1	mA
		M, D, L, R, F, G, H				4	
Schmitt Trigger	V_{T+}		1,2,3	All		4	V
	V_{T-}		1,2,3	All	1		
Hysteresis range 6/	V_{TH}		1,2,3	All	1.5	2	
Low level input voltage 7/	V_{IL}	TTL inputs 10/	1,2,3	All		0.8	
		CMOS, OSC inputs 10/				$0.3*V_{DD}$	
High level input voltage 7/	V_{IH}	TTL inputs 10/	1,2,3	All	2.2		
		CMOS, OSC inputs 10/			$0.7*V_{DD}$		
Input capacitance	C_I	V_{DD} = Open f = 1 MHz See 4.4.1c	4	All		15	pF
Output capacitance 5/	C_{O1}		4	All		15	
	C_{O2}		4	All		15	
	C_{O3}		4	All		17	
	C_{O4}		4	All		25	
Bidirect input/output capacitance 8/	C_{IO1}		4	All		16	
	C_{IO2}		4	All		20	
	C_{IO3}		4	All		26	
Functional tests 9/		V_{DD} = 5.5 V and 4.5 V See 4.4.1b	7,8	All			

See footnotes at end of table.

1/ Devices 01 -08 supplied to this drawing will meet all levels M, D, L, R, F, G and H of irradiation. However, devices 01 – 08 are only tested at the 'H' level. Devices 09 – 24 supplied to this drawing will meet all levels M, D, L, and R of irradiation. However, devices 09 - 24 are only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
2/ 4.5 V dc < V_{DD} < 5.5 V dc -55°C < T_C < 125°C, inputs are driven with V_{IL} maximum and V_{IH} minimum as specified in table I unless otherwise specified.
3/ V_{OL1} and V_{OH1} = TTL half-drive buffer.
V_{OL2} and V_{OH2} = TTL single-drive buffer.
V_{OL3} and V_{OH3} = TTL double-drive buffer.
V_{OL4} and V_{OH4} = TTL triple-drive buffer.
V_{OL5} and V_{OH5} = CMOS outputs.
V_{OL6} and V_{OH6} = CMOS outputs (optional. If required, specify in the AID).
V_{OL7} and V_{OH7} = OSC outputs.
4/ I_{IN1} = TTL CMOS, and Schmitt inputs.
I_{IN2} = inputs with pull-down resistors.
I_{IN3} = inputs with pull-down resistors, OSC.
I_{IN4} = inputs with pull-up resistors.
I_{IN5} = inputs with pull-up resistors, OSC.
5/ I_{OZ1}, I_{OS1}, and C_{01} = TTL half-drive buffer.
I_{OZ2}, I_{OS2}, and C_{02} = TTL single-drive, CMOS, OSC buffer.
I_{OZ3}, I_{OS3}, and C_{03} = TTL double-drive buffer.
I_{OZ4}, I_{OS4}, and C_{04} = TTL triple-drive buffer.
6/ Supplied as a design limit but not guaranteed or tested.
7/ V_{IL} and V_{IH} threshold levels are verified by performance of a low switching noise functional test or a dc V_{IL}/V_{IH} NAND-TREE test pattern.
8/ C_{IO1} = TTL single-drive, CMOS, OSC buffer.
C_{IO2} = TTL double-drive buffer.
C_{IO3} = TTL triple-drive buffer.
9/ Functional tests are conducted in accordance with MIL-STD-883, method 5004 with the following input test conditions: V_{IH} = V_{IH}(min) +20%, -0%; V_{IL} = V_{IL}(max) =0%, -50% as specified herein for TTL and CMOS compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
10/ CMOS levels only tested on CMOS devices, TTL levels only tested on TTL devices.

TABLE IB. SEP test limits . 1/ 2/

Device Type	T_A = Temperature ±10°C 3/	V_{CC} = 4.5 V		Bias for latch-up test V_{CC} = 5.5 V no latch-up LET = 3/
		Effective LET no upsets [MEV/(mg/cm^2)]	Maximum device cross section (μm^2) (LET = 120)	
All	+25°C	4/	4/	4/

NOTE: Devices that contain cross coupled resistance must be tested at the maximum rated T_A.
1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature T_A = +125°C.
4/ When characterized as a result of the procuring activities request, this parameter will be specified.

Case 4

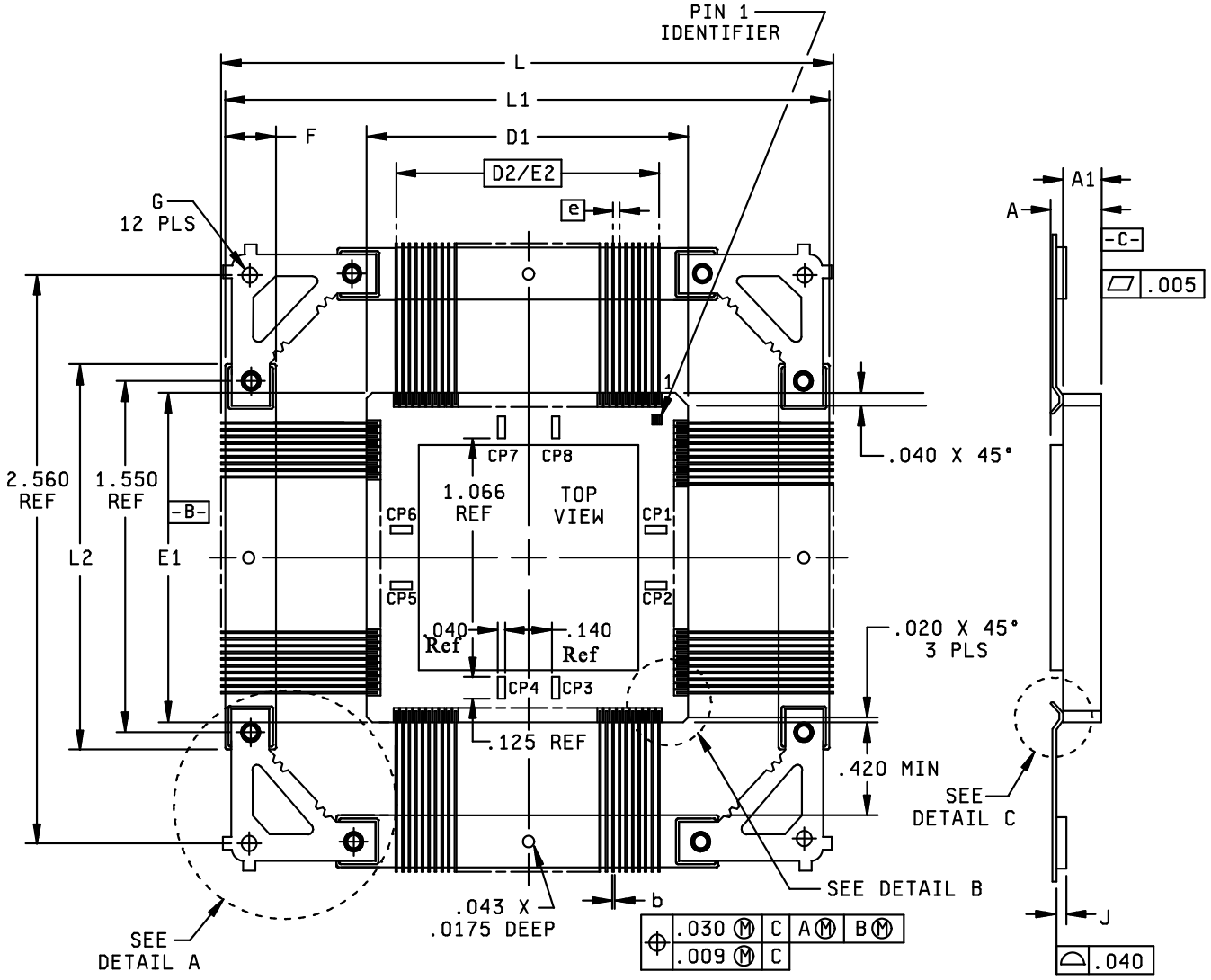
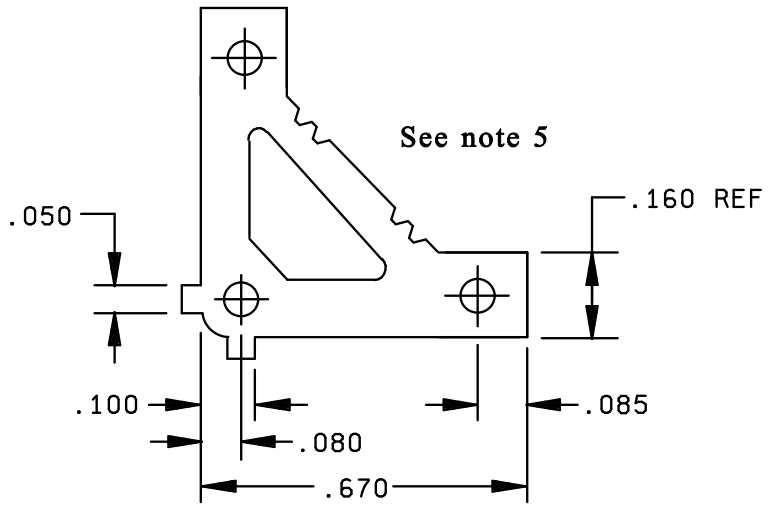
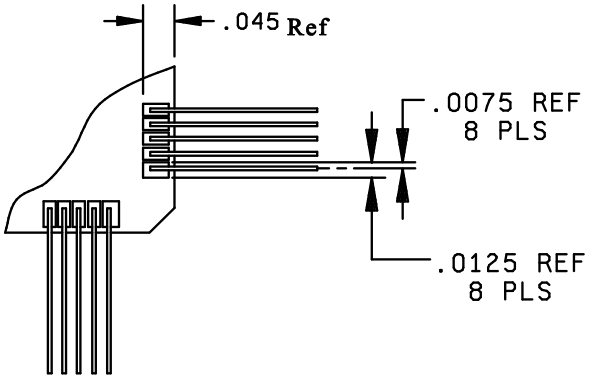


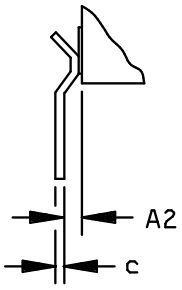
FIGURE 1. Case outline.



DETAIL A



DETAIL B



DETAIL C

FIGURE 1. Case outline -Continued.

Case 4

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.302		0.130
A1		2.667		0.105
A2	0.051	0.356	0.002	0.014
b	0.152	0.254	0.006	0.010
c	0.127	0.203	0.005	0.008
D1/E1	36.703	37.465	1.445	1.475
D2/E2	6.604 BSC		1.260 BSC	
e	0.508		0.020 BSC	
F		5.080		0.200
J	0.762	1.016	0.030	0.040
L		72.898		2.870
L1	69.850	70.358	2.750	2.770
L2		45.212		1.780

Capacitance Pads as located on top of package

CP1	VDD	CP5	VDD
CP2	VSS	CP6	VSS
CP3	VDDQ	CP7	VDDQ
CP4	VSSQ	CP8	VSSQ

Notes:

1. All exposed metalized areas are gold plated over nickel plating.
2. Capacitor mounting pads are dimensioned for an AVX/MIL-C-55681, P/N CDR05, 50 V 0.1 Φf chip capacitor.
3. Capacitor mounting pads labeled VSS, VDD, VSSQ, or VDDQ are connected to their respective internal ground or power planes.
4. The lid is electrically connected to VSS.
5. These areas may have notches and tabs different than shown.

FIGURE 1. Case outline -Continued.

Case N

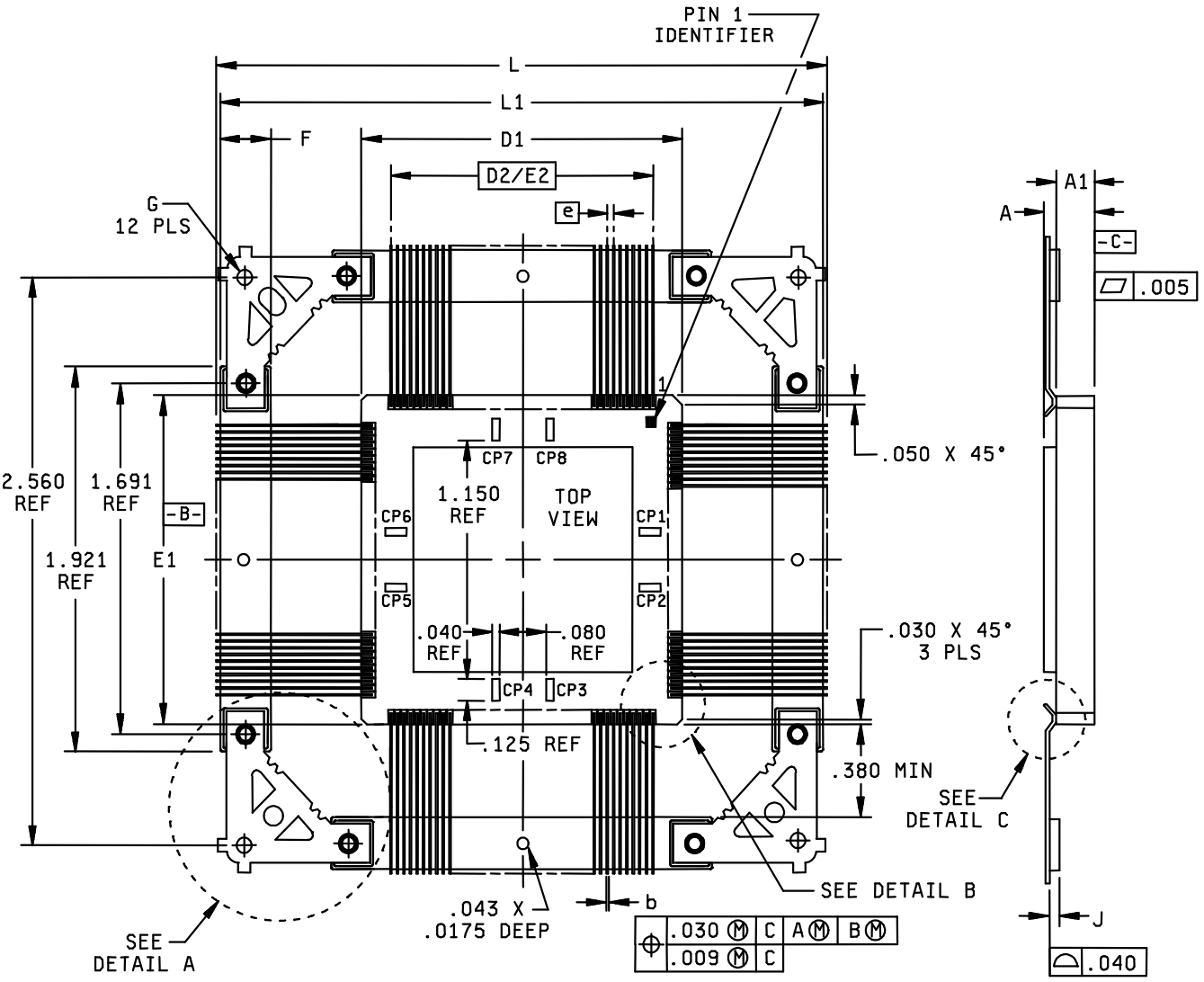


FIGURE 1. Case outline -Continued.

Case N

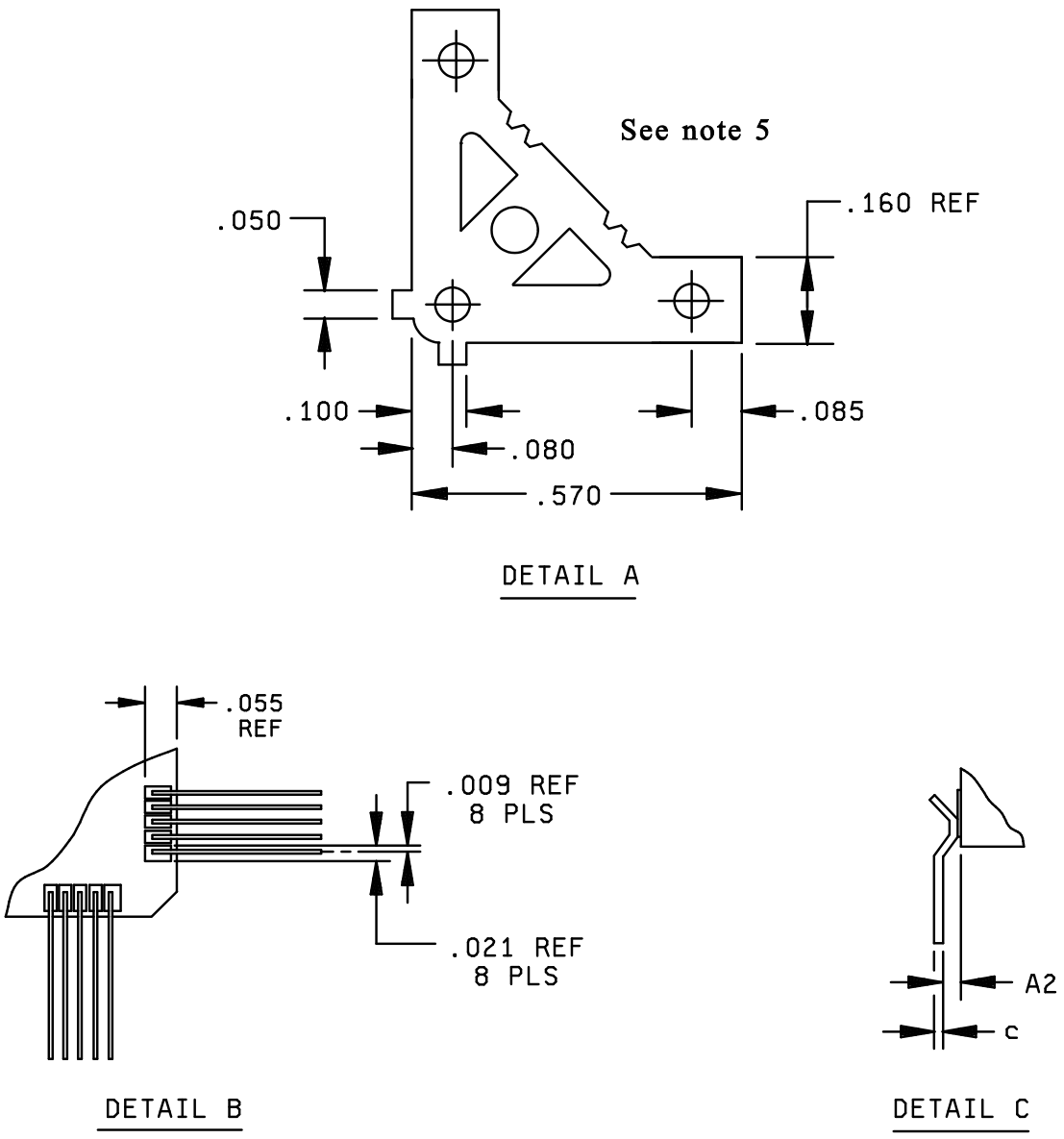


FIGURE 1. Case outline -Continued.

Case N

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.302		0.130
A1		2.667		0.105
A2	0.051	0.356	0.002	0.014
b	0.152	0.254	0.006	0.010
c	0.127	0.203	0.005	0.008
D1/E1	38.354	39.116	1.510	1.540
D2/E2	34.925 BSC		1.375 BSC	
e	0.635		0.025 BSC	
F		5.080		0.200
J	0.762	1.016	0.030	0.040
L		72.898		2.870
L1	69.850	70.358	2.750	2.770
L2		48.793		1.921

Capacitance Pads as located on top of package

CP1	VDD	CP5	VDD
CP2	VSS	CP6	VSS
CP3	VDDQ	CP7	VDDQ
CP4	VSSQ	CP8	VSSQ

Notes:

1. All exposed metalized areas are gold plated over nickel plating.
2. Capacitor mounting pads are dimensioned for an AVX/MIL-C-55681, P/N CDR05, 50 V 0.1 Φf chip capacitor.
3. Capacitor mounting pads labeled VSS, VDD, VSSQ, or VDDQ are connected to their respective internal ground or power planes.
4. The lid is electrically connected to VSS.
5. These areas may have notches and tabs different than shown.

FIGURE 1. Case outline -Continued.

Case 5

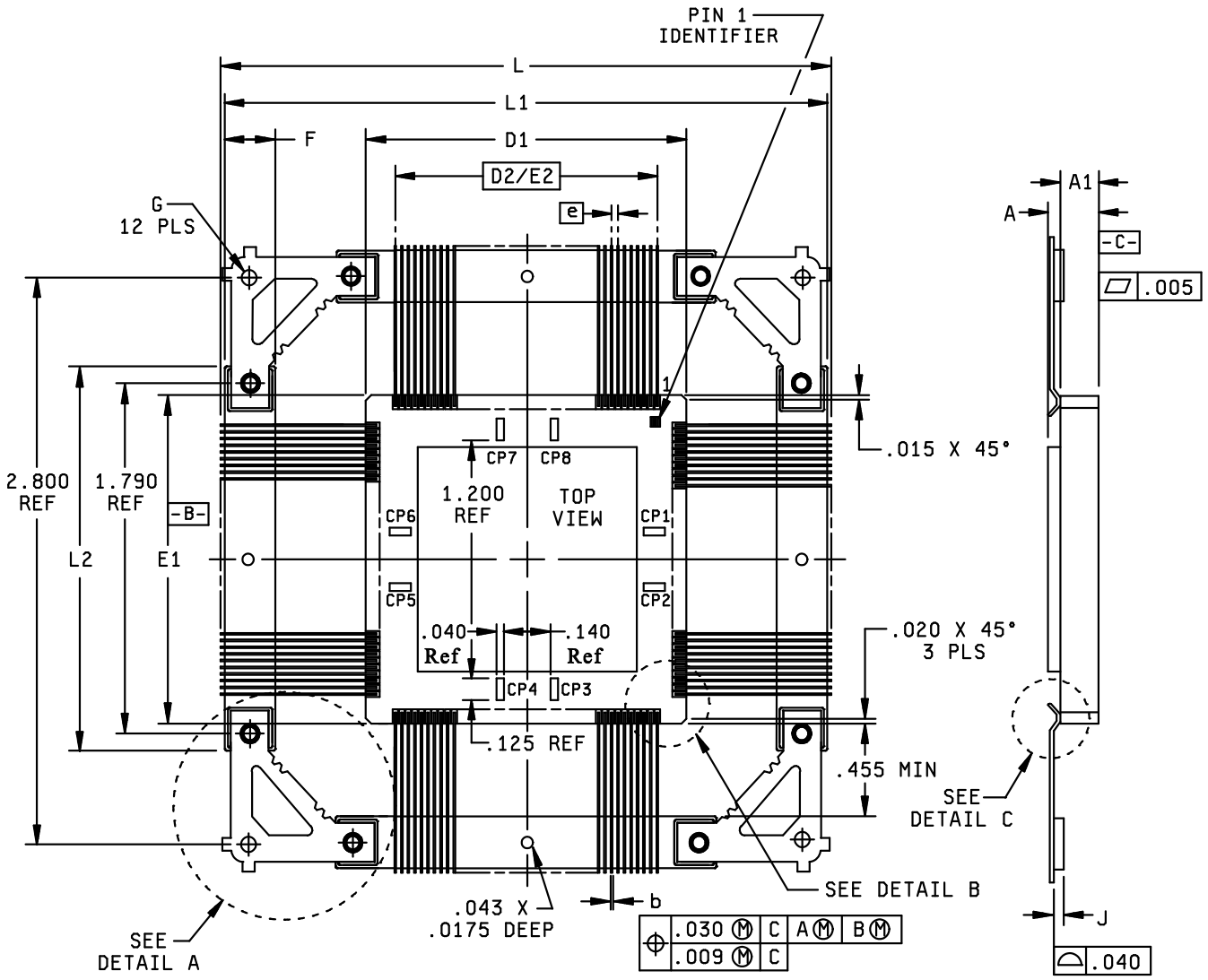
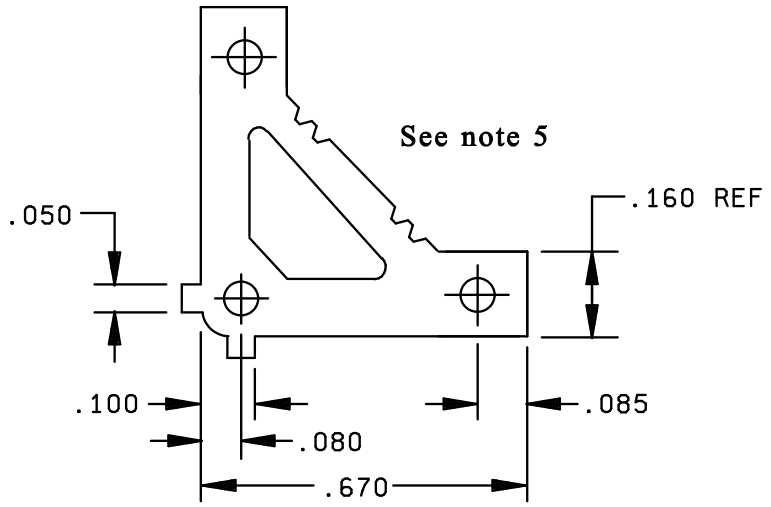
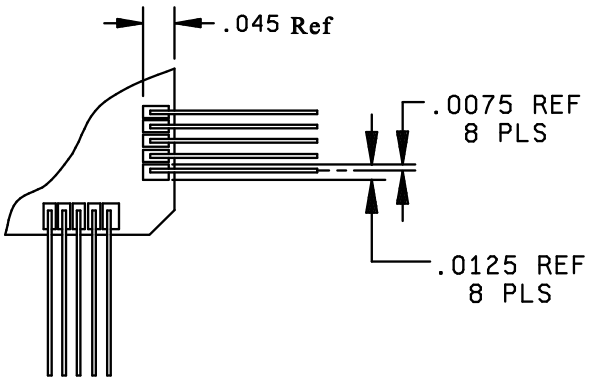


FIGURE 1. Case outline -Continued.

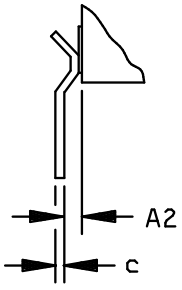
Case 5



DETAIL A



DETAIL B



DETAIL C

FIGURE 1. Case outline -Continued.

Case 5

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.302		0.130
A1		2.667		0.105
A2	0.051	0.356	0.002	0.014
b	0.152	0.254	0.006	0.010
c	0.127	0.203	0.005	0.008
D1/E1	41.529	42.291	1.635	1.665
D2/E2	34.925 BSC		1.500 BSC	
e	0.508		0.020 BSC	
F		5.080		0.200
J	0.762	1.016	0.030	0.040
L		77.978		3.070
L1	75.946	76.454	2.990	3.010
L2		51.308		2.020

Capacitance Pads as located on top of package

CP1	VDD	CP5	VDD
CP2	VSS	CP6	VSS
CP3	VDDQ	CP7	VDDQ
CP4	VSSQ	CP8	VSSQ

Notes:

1. All exposed metalized areas are gold plated over nickel plating.
2. Capacitor mounting pads are dimensioned for an AVX/MIL-C-55681, P/N CDR05, 50 V 0.1 Φf chip capacitor.
3. Capacitor mounting pads labeled VSS, VDD, VSSQ, or VDDQ are connected to their respective internal ground or power planes.
4. The lid is electrically connected to VSS.
5. These areas may have notches and tabs different than shown.

FIGURE 1. Case outline -Continued.

Open	V_{DD} = 5 V ∀ 0.5 V	GND
A2-A8, A10, A12, A13, A15-A18, B2-B4, B6-B13, B15, B16, B18, C6-C17, D2, D6-D12, D17, E1, E7-E9, F1-F3, F14, F16-F18, G1-G5, G14-G18, H1-H4, H14-H18, J2-J4, J14, J15, J17, J18, K1-K4, K17, L2-L4, L15-L17, M1-M4, M15-M18, N1-N3, N15-N18, P3, P7, P17, P18, R2, R7-R12, R17, R18, T7-T15, T18, U6-U17, V4-V7, V9, V11, V12, V14, V15	A1, A9, A11, B1, B17, C1-C3, C18, D1, D3, D16, D18, E4, E15, E18, F4, F5, F15, H5, J1, J5, K15, K16, K18, L1, L5, L14, L18, M5, M14, N5, N14, P2, P4, P6, P8-P10, P12, P13, P16, R1, R3-R6, R14-R16, T1-T5, U1-U4, V1-V3, V8, V10, V17, V18	A14, B5, B17, C5, D13, E2, E3, E10, E12, E16, E17, J16, N4, P1, P15, R13, T6, T16, T17, U5, U18, V13, V16
V_{DD} External Pin	GND External	
F8, F10, F12, G6, H13, J6, K13, L6, M13, N7, N9, N11	F7, F9, F11, G13, H6, J13, K6, L13, M6, N8, N10, N12	

Notes:

1. Each pin except F7, F8, F10, F11, F12, G6, G13, H6, H13, J6, J13, K6, K13, L6, L13, M6, M13, N7, N8, N9, N10, N11, and N12 will have a resistor of 2.49K Ω ± 5% for irradiation.

2. The irradiation circuit provided is for the standard evaluation circuit.

FIGURE 2. Radiation exposure circuit

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_I, C_O, and C_{IO} measurements) shall be measured only for the initial test and after process or design changes, which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

Table IIB. Delta limits

Parameter	Condition	LImits
I_{DDQ}	T_A = 25°C	±10% of measured value or 35 μA whichever is greater

Note: If device is tested at or below 35 μA no deltas are required. Delta's are performed at room temperature.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-PRF-38535 and MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IB herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (See 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be as required in MIL-PRF-38535. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60E to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

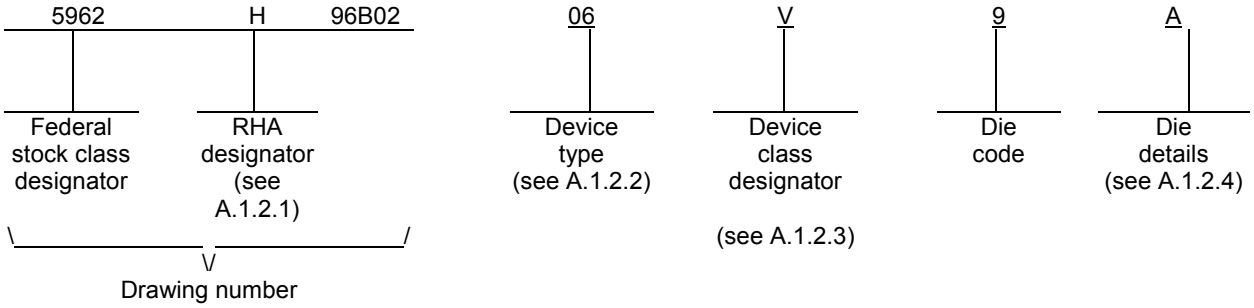
d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Circuit (total number of usable gates)	Array family
06	35,000 usable gates	UT35E/R

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
06	A-6

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
06	A-6

A.1.2.4.3 Interface materials.

Die type	Figure number
06	A-6

A.1.2.4.4 Assembly related information.

Die type	Figure number
06	A-6

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of the specification, standard, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-6.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-6.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-6.

A.3.2.5 Truth table(s). The truth table(s) shall be as defined in paragraph 3.2.3 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 QUALITY ASSURANCE PROVISIONS

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph A.3.4 herein).

c) 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883 test method 2010 or the alternate procedures allowed in MIL-STD-883 test method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

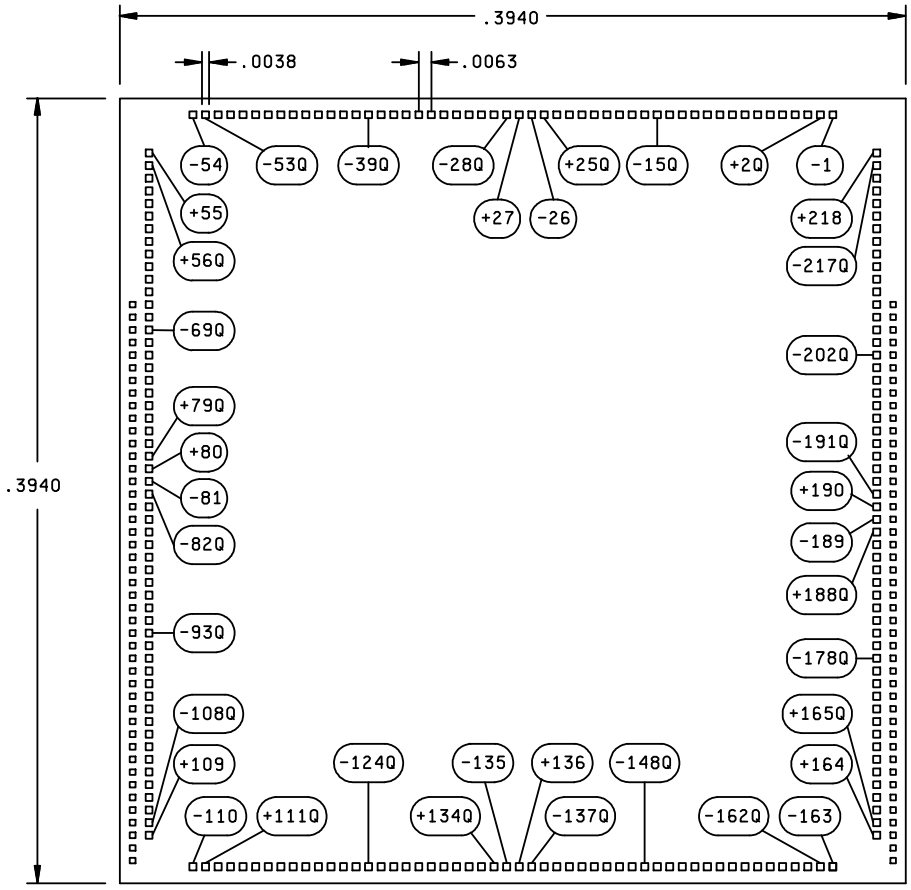
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.



Notes:
1. Die bondpad numbers are for reference only.
2. All die bonpads are to be wirebonded.
3. When required, JTAG ueses die pad 129, 130, 131, 132, and 133. Die pad 99 is ACO. Die pad 100 is ACI. Die pad 212 is used for buffer set-up at probe.

FIGURE A-6. Die bonding pad locations and electrical functions.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 394 x 394 mils
Die thickness: 17.5 ± 1 mils

Interface materials.
Top metallization: Silicon + Aluminum + Copper 9000 – 12500 Angstroms
Backside metallization: None: Backgrid

Glassivation.
Type: PSG
Thickness: 10000 ± 2000 Angstroms

Substrate: Single crystal silicon

Assembly related information.
Substrate potential: EPI on single crystall silicon
Special assembly instructions: None

Pads Location

ID	X	Y
1	165.0	185.9
2	158.7	185.9
3	152.4	185.9
4	146.1	185.9
5	139.8	185.9
6	133.5	185.9
7	127.2	185.9
8	120.9	185.9
9	114.6	185.9
10	108.3	185.9
11	102.0	185.9
12	95.7	185.9
13	89.4	185.9
14	83.1	185.9
15	76.8	185.9
16	70.5	185.9
17	64.2	185.9
18	57.9	185.9
19	51.6	185.9
20	45.3	185.9

FIGURE A-6. Die bonding pad locations and electrical functions - Continued.

ID	X	Y
21	39.0	185.9
22	32.7	185.9
23	26.4	185.9
24	20.1	185.9
25	13.8	185.9
26	7.5	185.9
27	1.2	185.9
28	-5.1	185.9
29	-11.4	185.9
30	-17.7	185.9
31	-24.0	185.9
32	-30.3	185.9
33	-36.6	185.9
34	-42.9	185.9
35	-49.2	185.9
36	-55.5	185.9
37	-61.8	185.9
38	-68.1	185.9
39	-74.4	185.9
40	-80.7	185.9
41	-87.0	185.9
42	-93.3	185.9
43	-99.6	185.9
44	-105.9	185.9
45	-112.2	185.9
46	-118.5	185.9
47	-124.8	185.9
48	-131.1	185.9
49	-137.4	185.9
50	-143.7	185.9
51	-150.0	185.9
52	-156.3	185.9
53	-162.6	185.9

ID	X	Y
54	-168.9	185.9
55	-184.6	170.2
56	-184.6	163.9
57	-184.6	157.4
58	-184.6	151.1
59	-184.6	144.8
60	-184.6	138.5
61	-184.6	132.2
62	-184.6	125.9
63	-184.6	119.6
64	-184.6	113.3
65	-184.6	107.1
66	-184.6	100.8
67	-184.6	94.5
68	-184.6	88.2
69	-184.6	81.9
70	-184.6	75.6
71	-184.6	69.3
72	-184.6	63.0
73	-184.6	56.7
74	-184.6	50.4
75	-184.6	44.1
76	-184.6	37.8
77	-184.6	31.5
78	-184.6	25.2
79	-184.6	18.9
80	-184.6	12.6
81	-184.6	6.3
82	-184.6	0.0
83	-184.6	-6.3
84	-184.6	-12.6
85	-184.6	-18.9
86	-184.6	-25.2

FIGURE A-6. Die bonding pad locations and electrical functions - Continued.

ID	X	Y
87	-184.6	-31.5
88	-184.6	-37.8
89	-184.6	-44.1
90	-184.6	-50.4
91	-184.6	-56.7
92	-184.6	-63.0
93	-184.6	-69.3
94	-184.6	-75.6
95	-184.6	-81.9
96	-184.6	-88.2
97	-184.6	-94.5
98	-184.6	-100.8
99	-184.6	-107.1
100	-184.6	-113.4
101	-184.6	-119.7
102	-184.6	-126.0
103	-184.6	-132.3
104	-184.6	-138.6
105	-184.6	-144.9
106	-184.6	-151.2
107	-184.6	-157.5
108	-184.6	-164.0
109	-184.6	-170.3
110	-168.9	-186.0
111	-162.6	-186.0
112	-156.3	-186.0
113	-150.0	-186.0
114	-143.7	-186.0
115	-137.4	-186.0
116	-131.1	-186.0
117	-124.8	-186.0
118	-118.5	-186.0
119	-112.2	-186.0

ID	X	Y
120	-105.9	-186.0
121	-99.6	-186.0
122	-93.3	-186.0
123	-87.0	-186.0
124	-80.7	-186.0
125	-74.4	-186.0
126	-68.1	-186.0
127	-61.8	-186.0
128	-55.5	-186.0
129	-49.2	-186.0
130	-42.9	-186.0
131	-36.6	-186.0
132	-30.3	-186.0
133	-24.0	-186.0
134	-17.7	-186.0
135	-11.4	-186.0
136	-5.1	-186.0
137	1.2	-186.0
138	7.5	-186.0
139	13.8	-186.0
140	20.1	-186.0
141	26.4	-186.0
142	32.7	-186.0
143	39.0	-186.0
144	45.3	-186.0
145	51.6	-186.0
146	57.9	-186.0
147	64.2	-186.0
148	70.5	-186.0
149	76.8	-186.0
150	83.1	-186.0
151	89.4	-186.0
152	95.7	-186.0

FIGURE A-6. Die bonding pad locations and electrical functions - Continued.

ID	X	Y
153	102.0	-186.0
154	108.3	-186.0
155	114.6	-186.0
156	120.9	-186.0
157	127.2	-186.0
158	133.5	-186.0
159	139.8	-186.0
160	146.1	-186.0
161	152.4	-186.0
162	158.7	-186.0
163	165.0	-186.0
164	180.7	-170.3
165	180.7	-163.8
166	180.7	-157.5
167	180.7	-151.2
168	180.7	-144.9
169	180.7	-138.6
170	180.7	-132.3
171	180.7	-126.0
172	180.7	-119.7
173	180.7	-113.4
174	180.7	107.1
175	180.7	-100.8
176	180.7	-94.5
177	180.7	-88.2
178	180.7	-81.9
179	180.7	-75.6
180	180.7	-69.3
181	180.7	-63.0
182	180.7	-56.7
183	180.7	-50.4
184	180.7	-44.1
185	180.7	-37.8

ID	X	Y
186	180.7	-31.5
187	180.7	-25.2
188	180.7	-18.9
189	180.7	-12.6
190	180.7	-6.3
191	180.7	0.0
192	180.7	6.3
193	180.7	12.6
194	180.7	18.9
195	180.7	25.2
196	180.7	31.5
197	180.7	37.8
198	180.7	44.1
199	180.7	50.4
200	180.7	56.7
201	180.7	63.0
202	180.7	69.3
203	180.7	75.6
204	180.7	81.9
205	180.7	88.2
206	180.7	94.5
207	180.7	100.8
208	180.7	107.1
209	180.7	113.4
210	180.7	119.7
211	180.7	126.0
212	180.7	132.3
213	180.7	138.6
214	180.7	144.9
215	180.7	151.2
216	180.7	157.6
217	180.7	163.9
218	180.7	170.2

FIGURE A-6. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-06-14

Approved sources of supply for SMD 5962-96B02 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard Microcircuit Drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN 3/
5962H96B0201Q_C	65342	UT25E/R_QCH
5962H96B0201V_C	65342	UT25E/R_VCH
5962H96B0202Q_C	65342	UT25E/R_QCH
5962H96B0202V_C	65342	UT25E/R_VCH
5962H96B0203Q_C	65342	UT25E/R_QCH
5962H96B0203V_C	65342	UT25E/R_VCH
5962H96B0204Q_C	65342	UT25E/R_QCH
5962H96B0204V_C	65342	UT25E/R_VCH
5962H96B0205Q_C	65342	UT25E/R_QCH
5962H96B0205V_C	65342	UT25E/R_VCH
5962H96B0206Q_C	65342	UT35E/R_QCH
5962H96B0206V_C	65342	UT35E/R_VCH
5962H96B0206Q9A	65342	UT35E/R_Q DIE
5962H96B0206V9A	65342	UT35E/R_V DIE
5962H96B0207Q_C	65342	UT75E/R_QCH
5962H96B0207V_C	65342	UT75E/R_VCH
5962H96B0208Q_C	65342	UT100E/R_QCH
5962H96B0208V_C	65342	UT100E/R_VCH
5962R96B0209Q_C	65342	UT25_QCR
5962R96B0209V_C	65342	UT25_VCR
5962R96B0210Q_C	65342	UT25_QCR
5962R96B0210V_C	65342	UT25_VCR
5962R96B0211Q_C	65342	UT25_QCR
5962R96B0211V_C	65342	UT25_VCR
5962R96B0212Q_C	65342	UT25_QCR
5962R96B0212V_C	65342	UT25_VCR

Standard Microcircuit Drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN 3/
5962R96B0213Q_C	65342	UT35_QCR
5962R96B0213V_C	65342	UT35_VCR
5962R96B0214Q_C	65342	UT75_QCR
5962R96B0214V_C	65342	UT75_VCR
5962R96B0215Q_C	65342	UT150_QCR
5962R96B0215V_C	65342	UT150_VCR
5962R96B0216Q_C	65342	UT200_QCR
5962R96B0216V_C	65342	UT200_VCR
5962R96B0217Q_C	65342	UT250_QCR
5962R96B0217V_C	65342	UT250_VCR
5962R96B0218Q_C	65342	UT300_QCR
5962R96B0218V_C	65342	UT300_VCR
5962R96B0219Q_C	65342	UT350_QCR
5962R96B0219V_C	65342	UT350_VCR
5962R96B0220Q_C	65342	UT400_QCR
5962R96B0220V_C	65342	UT400_VCR
5962R96B0221Q_C	65342	UT450_QCR
5962R96B0221V_C	65342	UT450_VCR
5962R96B0222Q_C	65342	UT500_QCR
5962R96B0222V_C	65342	UT500_VCR
5962R96B0223Q_C	65342	UT550_QCR
5962R96B0223V_C	65342	UT550_VCR
5962R96B0224Q_C	65342	UT600_QCR
5962R96B0224V_C	65342	UT600_VCR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability. Contact the listed approved source of supply for further information.
2/ Due to the nature of this SMD, the standard microcircuit drawing PIN and corresponding vendor similar PIN shall be specified in the AID. The vendor similar PIN will be based on the UTE/R gate array family. Contact the listed approved source of supply for availability of case outlines (defined in 1.2.4) for each device.
3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex UTMC Microelectronics System Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.